LTE Cat-1

Dual Band Module

CL32DAH31

Data Sheet

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Application

Restricted to M2M Device. *Not allowed for TELEMATICS use cases.

"M2M Device" hereinto is defined as a complete device that connects to network infrastructure equipment over a wireless network utilizing Wireless Wide-Area Network Standard through the module; utility metering devices, vending machines, cargo containers, ATM machines for electronic payment, remote monitoring systems, digital billboards, portable healthcare monitoring devices, alarm or security systems, portable tracking devices. Telephones and tablet devices are not included in the "M2M Devices".

● Revision History

Revision	Date	Summary of Change
Draft	2018.03.20	Draft version
1. 0	2019.01.22	Correction of errors
		Add Related Documents 3.5. UART Interface Update 1. introduction 3.1. pin 3.3. Signal Control Interface 3.4. USB Interface 3.9.1. RF Connector location 5.4.2. Power Consumption summary 6.1.1. Triggered by VBAT_L (VCC3 - VCC6) 6.1.2. Triggered by RESET pin 6.2. Host-Module Mutual Wakeup Interface for UART Table2-1, Table3-1, Table3-4, Table 4-2, Table 4-3, Table4-4, Table 4-5, Table 4-6, Table 4-7, Table 4-8, Table 4-9, Table4-10, Table5-4, Table5-6, Table9-1 Figure 2-1, Figure6-7, Figure6-8, Figure6-9, Figure6-10, Figure6-11, Figure7-3
1.1	2020.01.31	Update Related Documents 1. Introduction-Module highlights 3.4. USB Interface 6.1.1. Triggered by VBAT_L (VCC3 - VCC6) 6.1.2. Triggered by RESET pin Table2-1, Table3-1, Table 5-2, Table9-1
1.2	2020.04.09	Add Application

●Contents

● Related Documents

- Application Guide
- AT Commands Manual
- Circuit of EVB (recommended circuit)
- Evaluation Board Manual

1. Introduction

TAIYO YUDEN offers a turnkey solution of CAT-1 dual band LGA module supporting the following key features:

Module highlights

- Based on Altair Semiconductor ALT1160L chipset
- LTE CAT-1
- Supporting standard dual band design for docomo
  - 1 x Band19 (800MHz)
  - 1 x Band1 (2GHz)
- Small size (module size 26.0mm x 20.0 mm x 2.4 mm)
- Power supply: 2.3V-4.2V (VBAT_L) / 3.4V-4.2V (VBAT_H)
- Supports DRX, eDRX and standby ultra-low power consumption

LTE features highlights

- LTE CAT-1 support based on 3GPP release10 + eDRX
- Embedded IMS
- Embedded network processor

Features

- TCP/IP, UDP/IP, SSL/TLS 1.2, IPv4/IPv6 dual-stack, SMS, Power saving

Interface support

- USB2.0, 2/4 wires UART, GPIO

This document describes the hardware application interfaces and air interfaces that are provided when the module is used.
This document helps you to understand the interface specifications, electrical features and related product information of the module.

2. Overall Description

2.1. Function Overview

Table 2-1 Features

Feature	Description
Physical Features	Dimensions:26.0mm × 20.0mm × 2.4mm
Weight	2.8g
Operating Bands	LTE: FDD Band1,19, all bands with Rx diversity
Operating Temperature [1]	–30°C to +70°C
Storage Temperature	–40°C to +80°C
Power Voltage	VBAT_L: 2.3V to 4.2V [2] VBAT_H: 3.4V to 4.2V [2]
Application Interface (pin)	UIM_VCC (1.8V) pin
	USB2.0 (High-Speed)
	RESET pin
	VCC1-VCC6 pin
	WAKEUP_OUT pin
	WAKEUP_IN pin
	UART2 (2wires)
	UART1 (4wires)
SMS	Supports formats of PDU (AT command) SMS over SGs
Data Services	DL: 10Mbps (OFDMA) / UL: 5Mbps (SC-FDMA) [3]
Operating System	Linux

[1]: When the module works at this temperature, NOT all its RF specifications comply with the 3GPP RF specifications.

[2]: Power voltage of our evaluation board is as follows; VBAT_L: 3.0V
VBAT_H: 3.4V

[3]: the maximum value in theory

NOTE

● Use external interface for debugging and rewriting FW.

2.2. Circuit Block Diagram

2.2.1. Circuit Block Diagram

Figure 2-1 shows the circuit block diagram of the module. The application block diagram and major functional units of the module contain the following parts:

- Radio Frequency (RF) transceiver
- Multi-chip package (MCP) include power management unit
- RF Front End

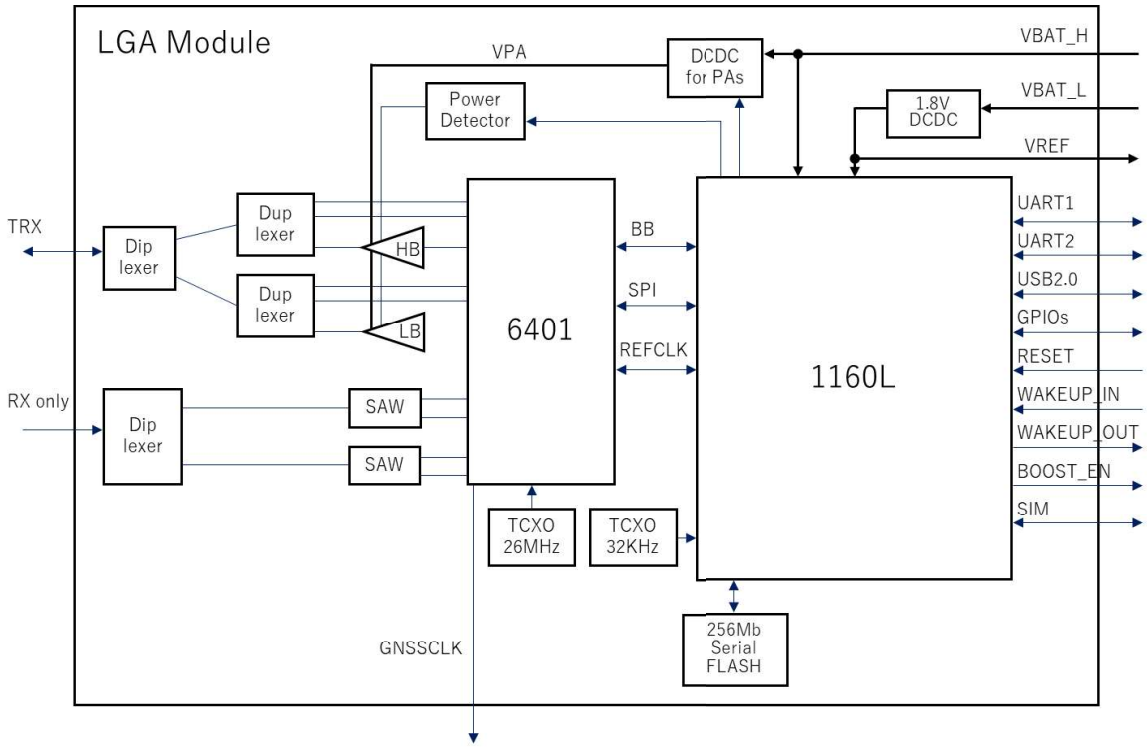


Figure 2-1 Circuit block diagram of the module

2.2.2. ALT1160L baseband

TAIYO YUDEN LGA module includes an integrated ALT1160L baseband.
A high-level block diagram of the baseband is shown in Figure 2-2.
The dotted line function in Figure 2-2 is not currently implemented.

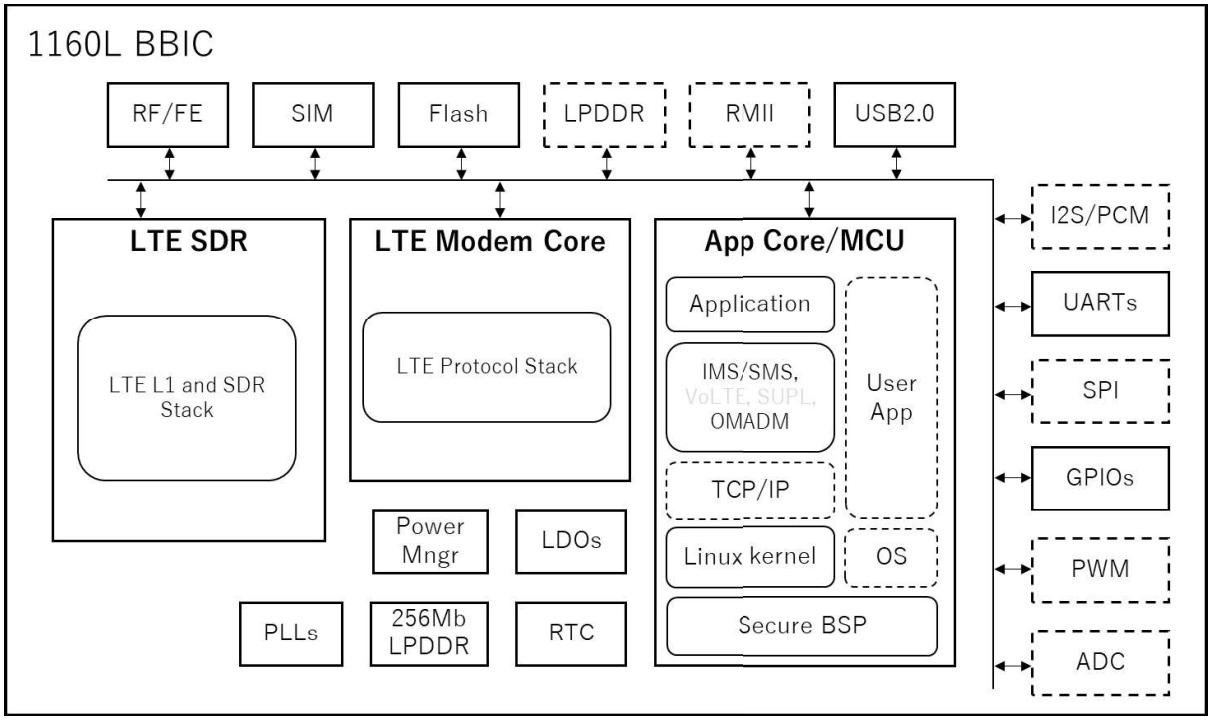


Figure 2-2 ALT1160L block diagram

2.2.3. ALT6401 RFIC

TAIYO YUDEN module includes an integrated ALT6401 RFIC. A RFIC block diagram of the baseband is shown in Figure 2-3. ALT6401 includes 3 bands support in the DL (1LB + 2HB) and 2 bands support in the UL (1LB + 1HB). ALT6401 has integrated power management module, so no external PMU is required.

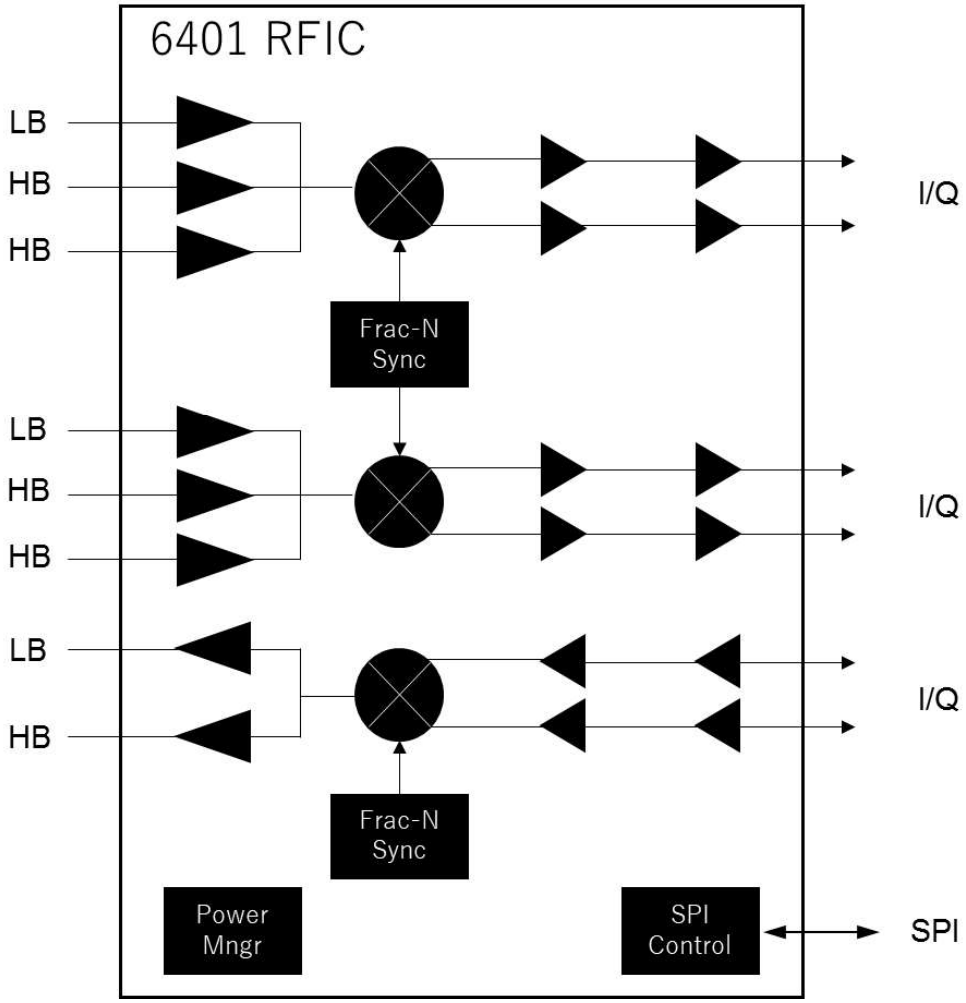


Figure 2-3 ALT6401 RFIC block diagram

3. Description of the Application Interfaces

3.1. pin

The module uses pins as its external interfaces.
Figure 3-1 shows an LGA map diagram of this module.
Table 3-1 shows definitions of pins on the LGA map.

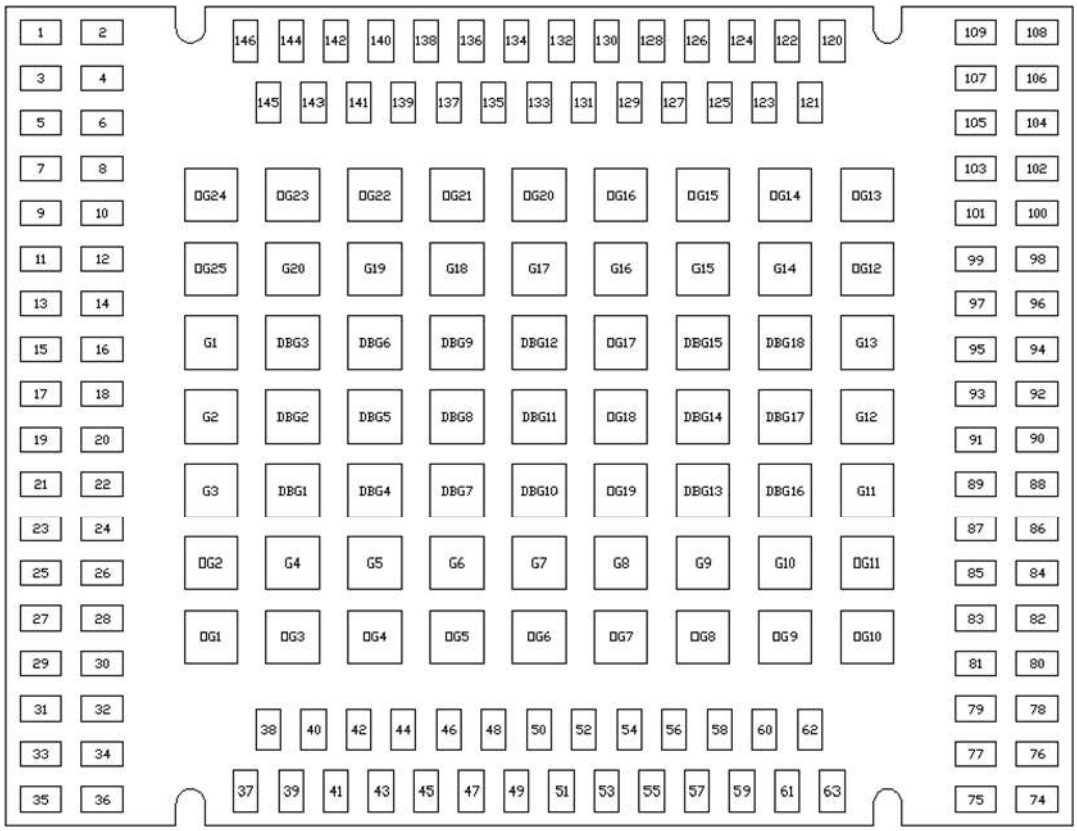


Figure 3-1 LGA map diagram (TOP_THRU_ VIEW)

Table 3-1 Definitions of pins

No.	Pin Name	Direction	Type	Recommendation for Unused pin	Description
1	GND	-	-	-	Ground
2	GND	-	-	-	Ground
3	NC	-	-	Open	Not connected. It is better to solder.
4	GND	-	-	-	Ground
5	GND	-	-	-	Ground
6	GND	-	-	-	Ground
7	GND	-	-	-	Ground
8	GND	-	-	-	Ground
9	NC	-	-	Open	Not connected. It is better to solder.
10	GND	-	-	-	Ground
11	GND	-	-	-	Ground
12	GND	-	-	-	Ground
13	GND	-	-	-	Ground
14	GND	-	-	-	Ground
15	RF_1	-	A	-	RF TRX, main LTE antenna
16	GND	-	-	-	Ground
17	GND	-	-	-	Ground
18	GND	-	-	-	Ground
19	GND	-	-	-	Ground
20	GND	-	-	-	Ground
21	RF_2	-	A	-	RF RX, RX only LTE antenna
22	GND	-	-	-	Ground
23	GND	-	-	-	Ground
24	GND	-	-	-	Ground
25	GND	-	-	-	Ground
26	GND	-	-	-	Ground
27	NC	-	-	Open	Not connected. It is better to solder.
28	GND	-	-	-	Ground
29	GND	-	-	-	Ground
30	GND	-	-	-	Ground
31	GND	-	-	-	Ground
32	GND	-	-	-	Ground

No.	Pin Name	Direction	Type	Recommendation for Unused pin	Description
33	NC	-	-	Open	Not connected. It is better to solder.
34	GND	-	-	-	Ground
35	GND	-	-	-	Ground
36	GND	-	-	-	Ground
37	VCC1	I	P	-	VBAT_L Power Module input power supply for internal 1.8V DC-DC. Module input voltage range 2.3V – 4.2V.
38	VCC2	I	P	-	
39	VCC3	I	P	-	VBAT_H Power Module input power supply for 1160L PMU and PA DC-DC. Module input voltage range 3.4V – 4.2V.
40	VCC4	I	P	-	
41	VCC5	I	P	-	
42	VCC6	I	P	-	
43	NC	-	-	Open	Not connected. It is better to solder.
44	GND	-	-	-	Ground
45	GND	-	-	-	Ground
46	GPIO3/PCM_FS	O	D, PD	Open	Reserved
47	GPIO2/PCM_DIN	I	D, PU	Open	Reserved
48	GPIO1/PCM_DOUT	O	D, PU	Open	Reserved
49	GPIO0/PCM_CLK	O	D, PD	Open	Reserved
50	GND	-	-	-	Ground
51	GND	-	-	-	Ground
52	RFFE_SCLK	O	D, PD	Open	Reserved
53	RFFE_SDATA	IO	D, PD	Open	Reserved
54	GNSS_FREF_ EN	I	D, PD	Open	Reserved
55	FEM_CTRL2	IO	D, PD	Open	Reserved
56	GNSS_FREF_OUT	O	D	Open	Reserved
57	SAR_VAIN1	IO	D	Open	Reserved
58	SAR_VAIN0	IO	D	Open	Reserved
59	FEM_CTRL3	IO	D, PD	Open	Reserved
60	ALARMZ	O	A, PU (100kΩ)	Open	Output indication signal for power state: low = Active 1.8V = Hibernation

No.	Pin Name	Direction	Type	Recommendation for Unused pin	Description
61	RETLE_N_OUT	O	PD (10kΩ)	Open	Output indication signal for DDR retention state: 0V = not retention 1.8V = Active
62	VO3v15	O	P	-	3.15V power output, up to 100mA. This voltage shut down during hibernation.
63	EJTAG_TRST	I	D, PD	Open	Reserved
74	GND	-	-	-	Ground
75	GND	-	-	-	Ground
76	GPIO13/UART1_DTR	I	D, PD	Open	Reserved
77	GPIO15/UART1_RI	O	D, PD	Open	Reserved
78	GPIO16/UART1_DCD	O	D, PD	Open	Reserved
79	GPIO17/UART1_DSR	O	D, PD	Open	Reserved
80	UART1_CTS	I	D, PD	Open or Low	UART1 Clear to Send
81	UART1_RTS	O	D, PD	Open or Low	UART1 Ready to Send
82	UART1_RX	I	D, PU		UART1 receiving data - Input to the module. Host actives UART1_RX after sets WAKEUP_IN to high.
83	UART1_TX	O	D, PU		UART1 transmitting data - Output form the module. Host actives UART1_TX after sets WAKEUP_IN to high.
84	GND	-	-	-	Ground
85	GND	-	-	-	Ground
86	USB_Dp		A	-	USB2.0 Data positive
87	NC	-	-	Open	Not connected. It is better to solder.
88	USB_Dn		A	-	USB2.0 Data negative
89	GND	-	-	-	Ground
90	GND	-	-	-	Ground
91	GND	-	-	-	Ground
92	GPIO9 /SPIM_EN_2	O	D, PD	Open	Reserved
93	GPIO6 /SPI_S_CS	I	D, PU	Open	Reserved

No.	Pin Name	Direction	Type	Recommendation for Unused pin	Description
94	GPIO4/SPI_S_MISO	O	D, PD	Open	Reserved
95	GPIO8 /SPI_S_CLK	I	D, PD	Open	Reserved
96	GPIO5/SPI_S_MOSI	I	D, PD	Open	Reserved
97	SPIM_MOSI	O	D, PU	Open	Reserved
98	SPIM_CLK	O	D,PD	Open	Reserved
99	SPIM_EN_1	O	D, PD	Open	Reserved
100	SPIM_MISO	I	D, PU	Open	Reserved
101	GPIO7 /SPI_S_RDY	O	D, PD	Open	Reserved
102	TCK	I	D, PD	Open	Reserved
103	FEM_CTRL11	IO	D, PD	Open	Reserved
104	GND	-	-	-	Ground
105	GND	-	-	-	Ground
106	UART2_RX	I	D, PU	-	UART2 RX data
107	UART2_TX	O	D, PU	-	UART2 TX data
108	GND	-	-	-	Ground
109	GND	-	-	-	Ground
120	VDDIO1v8 _OUT	O	P	-	1.8V output, up to 50mA. This voltage shut down during Hibernation.
121	EXT_VREF	O	-	Open	external reference voltage input connected to internal LDO domain of 1160L
122	RSTN	I	PU (10kΩ)	Open	Reset the baseband chip. Reset input signal 0v = Reset, 1.8V = Active This pin is not used. Not connected.
123	SF_SI/IO0	IO	D	Open	Reserved
124	SF_CLK	O	D, PD	Open	Reserved
125	SF_n HOLD/IO3	IO	D, PD	Open	Reserved
126	SF_nWP/IO2	IO	D, PD	Open	Reserved
127	SF_SO/IO1	IO	D, NP	Open	Reserved
128	GPIO10/SF_nCS2	O	D, PU	Open	Reserved
129	TDO	O	D, PU	Open	Reserved
130	TDI	I	D, PD	Open	Reserved

No.	Pin Name	Direction	Type	Recommendation for Unused pin	Description
131	I2C_SCL	O	D, PU	Open	Reserved
132	2C_SDA	IO	D, PU	Open	Reserved
133	UIM_VCC	O	P		Output supply to SIM can be 1.8V
134	UIM_DATA	IO	D, PU		SIM IO If SIM latch is used the UIM_DATA is latched during Hibernation
135	UIM_CLK	O	D, PU		SIM CLK If SIM latch is used the UIM_CLK is latched during Hibernation
136	UIM_RESET	O	D, PU		SIM RSTt If SIM latch is used the UIM_RST is latched during Hibernation
137	UIM_DETECT	-	D, PD	Open	SIM card DETECT. Not assigned.
138	BOOST_EN		A, PD (100kΩ)	Open	Open drain output (Pch) 1.8V = enable the external boost DC-DC for VBAT_H power.
139	GND	-	-	-	Ground
140	GND	-	-	-	Ground
141	WWAN_STATE	O	D, PD	Open	Reserved
142	NC	-	-	Open	Not connected. It is better to solder.
143	WAKEUP_OUT/GPIO143	O	D, PD	Open	Output signal interrupt to wakeup HOST (GPIO143) May require using external pull down resistors if connected to the host.
144	WAKEUP_IN/GPIO144	I	D, PD	PD	Input signal to wakeup modem. Must keep stable and valid: 0V = modem can enter Hibernation 1.8V = wakeup the modem or keep active - module can't enter Hibernation. If sleep implementation not required this pin can used as GPIO (GPIO144).

No.	Pin Name	Direction	Type	Recommendation for Unused pin	Description
145	RESET	I	D, PU (100kΩ)	Open	HW_RESET Reset input signal to the module, has internal PU to 1.8V. 0V = Reset 1.8V = Active
146	VREF	O	P		Reference Logic Voltage. 1.8V output up to 50 mA. This voltage is always on.
G1	GND	-	-	-	Ground
G2	GND	-	-	-	Ground
G3	GND	-	-	-	Ground
G4	GND	-	-	-	Ground
G5	GND	-	-	-	Ground
G6	GND	-	-	-	Ground
G7	GND	-	-	-	Ground
G8	GND	-	-	-	Ground
G9	GND	-	-	-	Ground
G10	GND	-	-	-	Ground
G11	GND	-	-	-	Ground
G12	GND	-	-	-	Ground
G13	GND	-	-	-	Ground
G14	GND	-	-	-	Ground
G15	GND	-	-	-	Ground
G16	GND	-	-	-	Ground
G17	GND	-	-	-	Ground
G18	GND	-	-	-	Ground
G19	GND	-	-	-	Ground
G20	GND	-	-	-	Ground
DG1	GND	-	-	-	Ground
DG2	GND	-	-	-	Ground
DG3	GND	-	-	-	Ground
DG4	GND	-	-	-	Ground
DG5	GND	-	-	-	Ground
DG6	GND	-	-	-	Ground
DG7	GND	-	-	-	Ground
DG8	GND	-	-	-	Ground
DG9	GND	-	-	-	Ground

No.	Pin Name	Direction	Type	Recommendation for Unused pin	Description
DG10	GND	-	-	-	Ground
DG11	GND	-	-	-	Ground
DG12	GND	-	-	-	Ground
DG13	GND	-	-	-	Ground
DG14	GND	-	-	-	Ground
DG15	GND	-	-	-	Ground
DG16	GND	-	-	-	Ground
DG17	GND	-	-	-	Ground
DG18	GND	-	-	-	Ground
DG19	GND	-	-	-	Ground
DG20	GND	-	-	-	Ground
DG21	GND	-	-	-	Ground
DG22	GND	-	-	-	Ground
DG23	GND	-	-	-	Ground
DG24	GND	-	-	-	Ground
DG25	GND	-	-	-	Ground
DBG1	GND	-	-	-	Ground
DBG2	GND	-	-	-	Ground
DBG3	GND	-	-	-	Ground
DBG4	GND	-	-	-	Ground
DBG5	GND	-	-	-	Ground
DBG6	GND	-	-	-	Ground
DBG7	GND	-	-	-	Ground
DBG8	GND	-	-	-	Ground
DBG9	GND	-	-	-	Ground
DBG10	GND	-	-	-	Ground
DBG11	GND	-	-	-	Ground
DBG12	GND	-	-	-	Ground
DBG13	GND	-	-	-	Ground
DBG14	GND	-	-	-	Ground
DBG15	GND	-	-	-	Ground
DBG16	GND	-	-	-	Ground
DBG17	GND	-	-	-	Ground
DBG18	GND	-	-	-	Ground

NOTE

- **I:** Input only functionality. **O:** Output only functionality.
  IO: Both input and output functionality.
- **A:** Analog pin. **D**: Digital pin. **PD:** Pull Down. **PU:** Pull Up. **P**: Power.
- Connected to a common ground plane.
- VREF (pin 146): see 3.6. GPIO pins.

3.2. Power Management Unit (PMU)

3.2.1. Overview

ALT1160L contains a PMU unit that is responsible for the power supply of all the different voltage needed for the ALT1160L functional behavior and the functionality of a neighbor chip (The RFIC can get power supplies from the ALT1160L). The PMU is an integration of an external PMIC into the IC.

The power supply part of the module contains:

- RTC (Real Time Clock)
- APC (Advance Power Controller)
- different regulators (LDOs and DC-DC)

Table 3-2 lists the definitions of the pins on the power supply interface

Pin No.	Signal Name	I/O	Description	voltage (V)
37	VCC1	I	VBAT_L Module input power supply for internal 1.8V DC-DC.	2.3 - 4.2
38	VCC2	I		
39	VCC3	I	VBAT_H Module input power supply for 1160L PMU and PA DC-DC.	3.4 - 4.2
40	VCC4	I		
41	VCC5	I		
42	VCC6	I		
62	V0315	O	3.15V output, up to 100mA.	3.15
133	UIM_VCC	O	Output supply to SIM can be 1.8V configurable by software.	1.8
146	VREF	O	1.8V output to 50mA. This voltage is always on.	1.8

3.2.2. Power Supply VBAT_L (VCC1 - VCC2) and VBAT_H (VCC3 - VCC6)

There are two types of VBAT of the module.

(1) VBAT_L (VCC1 - VCC2)

VBAT_L is the power supply of RTC and LPDDR.

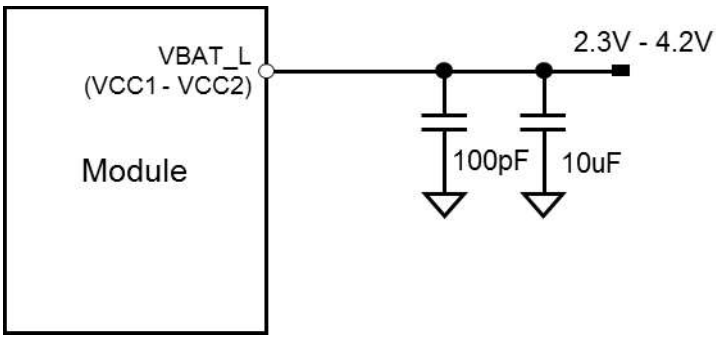


Figure 3-2 VBAT_L (VCC1 - VCC2) supply block diagram

(2) VBAT_H (VCC3 - VCC6)

VBAT_H is the power supply to be controlled synchronously with the DRX /eDRX cycle.
See following page for details.

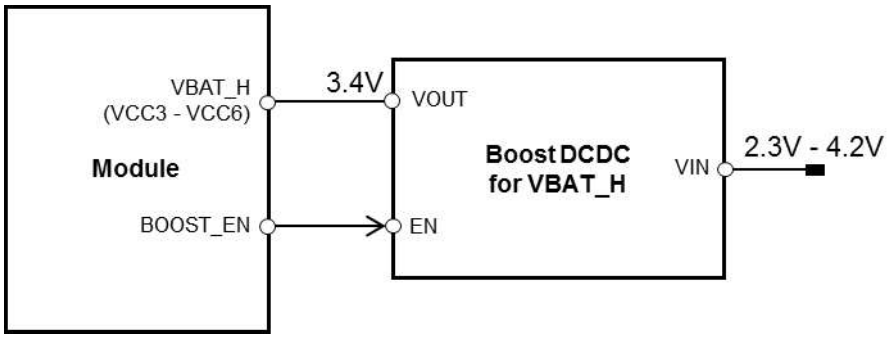


Figure 3-3 VBAT_H (VCC3 - VCC6) supply block diagram

When VBAT_L is 2.3V (minimum value), must keep 2.2V or more, during Tx.

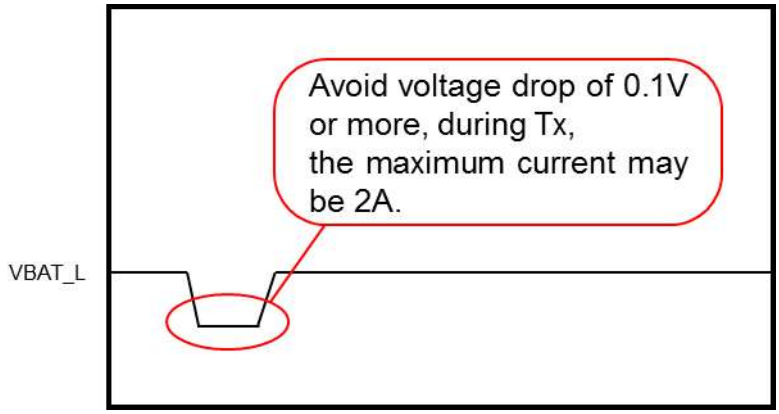


Figure 3-4 Drop of power supply voltage (VBAT_L)

When VBAT_H is 3.4V (minimum value), must keep 3.2V or more, during Tx.

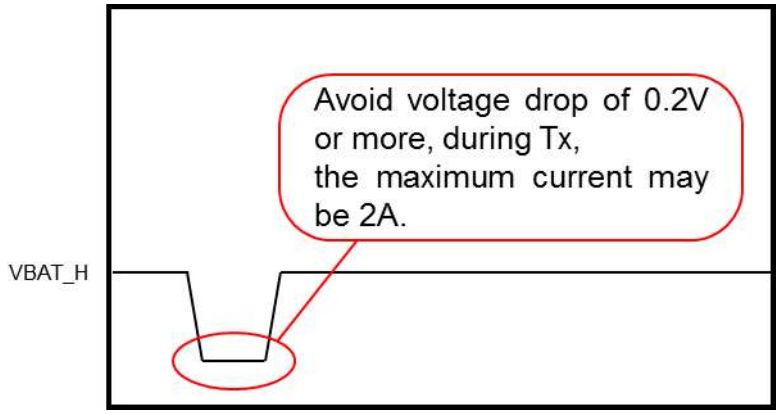


Figure 3-5 Drop of power supply voltage (VBAT_H)

After turning off the power and wait 100ms or more, next turning on the power supply.

Figure 3-6 shows reference block diagram of the module.
An external DC-DC converter is required on the VBAT_H side of the module.
The reason why the DC-DC converter is necessary is as follows.

- It is synchronizing with eDRX, for power saving.
- The module learns autonomously eDRX cycle.
  BOOST_EN synchronizes with eDRX and can control the DC-DC converter.
  (BOOST_EN control VBAT_H in synchronization with eDRX.)

Figure 3-6 is the recommended circuit. We designed to minimize reduce the current consumption during Hibernation.

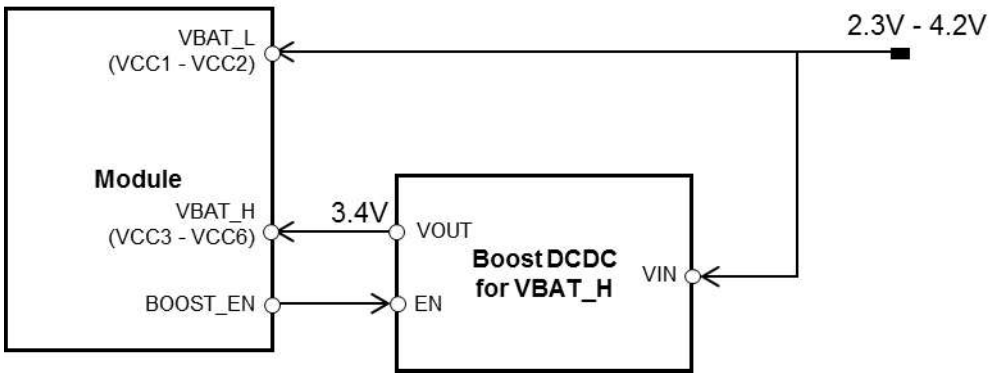


Figure 3-6 Reference power block diagram of the module

The external Boost DC-DC is TPS61021ADSG.
VBAT_H (VCC3 - VCC6) should be supplied by external Boost DC-DC (set to 3.4V) and controlled by BOOST_EN pin.
Figure 3-7 shows circuit of the DC-DC.
Refer to datasheet of TPS61021ADSG for details.

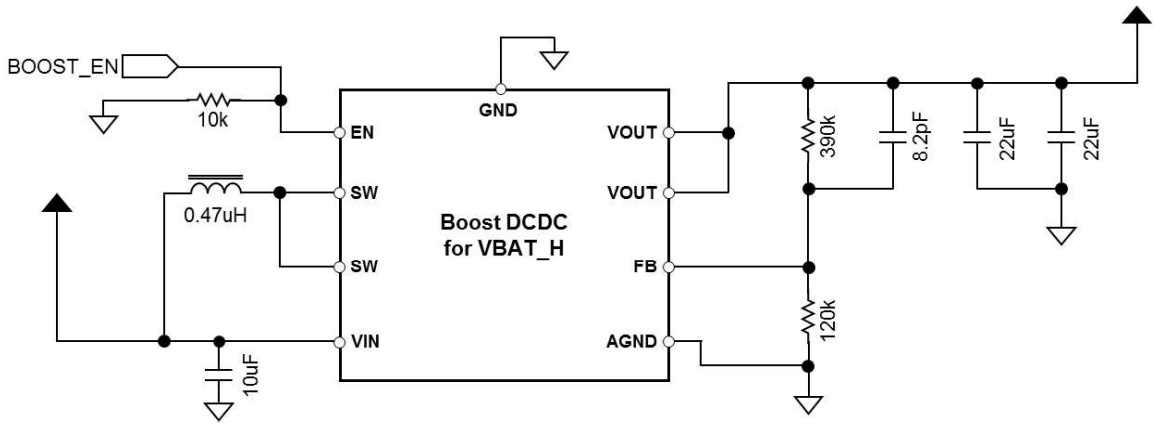


Figure 3-7 Reference circuit of the DC-DC

3.2.3. USIM Power Output UIM_VCC

Through the UIM_VCC power supply interface, 1.8V power from the module can be supplied to UIM card.
Special attention should be taken on PCB design at the host side.

3.3. Signal Control Interface

3.3.1. Overview

The signal control part of the interface in the module contains the following:

- RESET pin
- WAKEUP_OUT pin
- WAKEUP_IN pin
- RSTN pin
- BOOST_EN pin
- ALARMZ pin
- RETLE_N_OUT pin

Table 3-3 Pins on the signal control interface

Pin No.	PIN Name	I/O	Description
145	RESET	I	Reset input signal to the module, has internal PU to 1.8V. Must keep stable and valid. 0V = Reset 1.8V = Active
143	WAKEUP_OUT	O	Output signal interrupt to wakeup HOST.
144	WAKEUP_IN	I	Input signal to wakeup modem. Must keep stable and valid. 0V = modem can enter Hibernation 1.8V = wakeup the modem or keep active - module won't enter Hibernation if this signal kept high
122	RSTN	I	Reset input signal. The pin is not used. Not connected.
138	BOOST_EN		Open drain output (Pch) 1.8V = enable the external boost DC-DC for VBAT_H power.
60	ALARMZ		Output indication signal for power state. low = Active 1.8V = Hibernation
61	RETLE_N_OUT	O	Output indication signal for Hibernation. 0V = Hibernation 1.8V = Active

3.3.2. RESET Pin

Reset input signal to the module, has internal PU to 1.8V.
Pulling RESET low more than 100ms and then pulling high will reset the module.

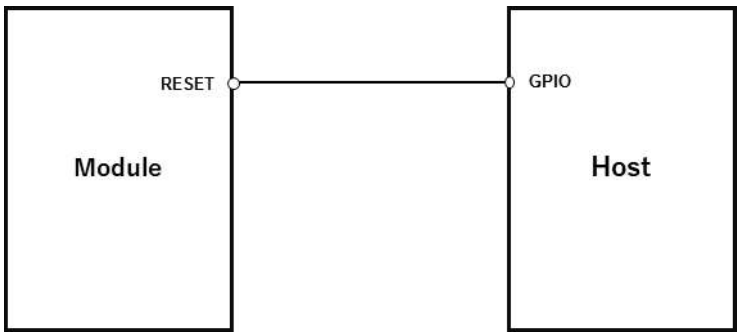


Figure 3-8 Connections of the RESET Pin

3.3.3. WAKEUP_OUT Pin

Table 3-4 Two States of WAKEUP_OUT

Item	Pin state	Description
1	High	Interrupt to wakeup HOST. Module wants to send data to host.
2	Low	No interrupt. May require using external pull down resistors if connected to the host.

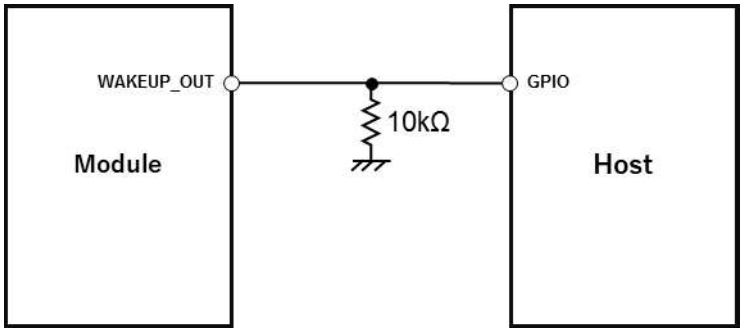


Figure 3-9 Connections of the WAKEUP_OUT Pin

3.3.4. WAKEUP_IN Pin

Input signal to WAKEUP_IN must keep stable and valid.

Table 3-5 Two states of WAKEUP_IN

Item	Pin state	Description
1	High	Wakeup the module or keep active. Module won't enter Hibernation if this signal kept high. The pin is related to BOOST_EN pin.
2	Low	Change the state of module Active to Hibernation. Note: Never set WAKEUP_IN to low when the host will send data to the module. (See 6.2.3. Close data interface)

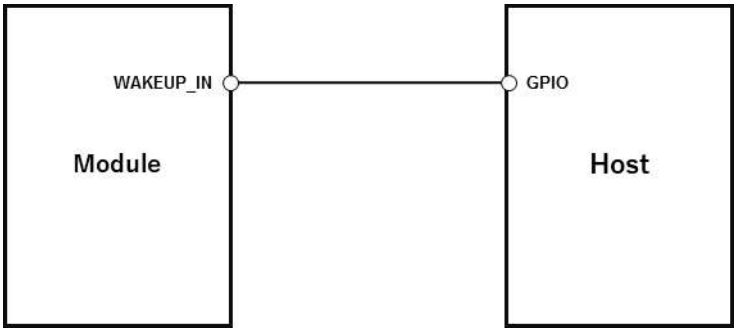


Figure 3-10 Connections of the WAKEUP_IN Pin

3.3.5. RSTN Pin

The pin is not used because it resets only the baseband chipset, not the module.
The pin should be opened.

3.3.6. BOOST_EN Pin

Open drain output (Pch) to enable the external boost DC-DC for VBAT_H power.
When host sets WAKEUP_IN to high, BOOST_EN is also to be high.
This pin synchronized with eDRX.

There are two reasons why the diode is present in Figure 3-11.
(1) To prevent output signal from BOOST_EN from being input to GPIO.
(To protect the GPIO of the host.)
(2) In order to wakeup VBAT_H along with WAKEUP_IN.
Even if only WAKEUP_IN is to be high, VBAT_H will not wake up and the module will not wake up.
When BOOST_EN is to be high along with WAKEUP_IN, VBAT_H wakes up and the module also wakes up.

Table 3-6 Two states of BOOST_EN

Item	Pin state	Description
1	High	Enable
2	Low	Disable

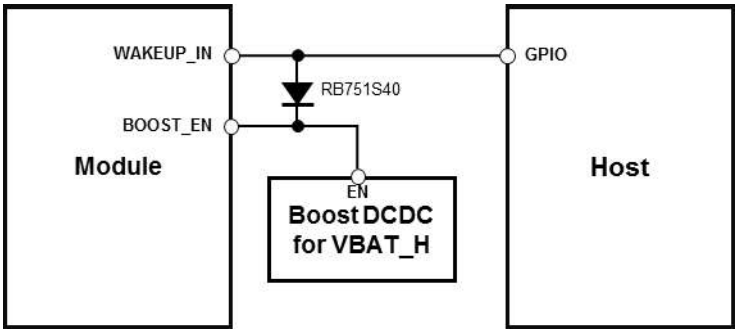


Figure 3-11 Connections of the BOOST_EN Pin

3.3.7. ALARMZ Pin

Output indication signal for power state.

Table 3-7 Two states of ALARMZ

Item	Pin state	Description
1	High	Hibernation
2	Low	Active

3.3.8. RETLE_N_OUT Pin

Output indication signal for Hibernation.

Table 3-8 Two states of RETLE_N_OUT

Item	Pin state	Description
1	High	Active
2	Low	Hibernation

3.4. USB Interface

The module is compliant with USB2.0 high speed protocol. The USB input/output lines are following USB2.0 specifications. (Maximum 480Mbps.)
It is for debug.

Table 3-9 List of USB pins

Pin No.	Pin Name	Description
86	USB_Dp	USB2.0 Data positive
88	USB_Dn	USB2.0 Data negative

3.5. UART Interface

The module includes a 4-wire (UART1) and 2-wire (UART2) UART interface.
UART interface is available for the communication with a host application processor (AT commands, data communication etc.). The UART is an asynchronous serial interface and UART1 is maximum baud rate of 3M Baud.

The baud rate can only be changed via AT command. (Refer to Software Application Guide)
Default setting is following:
Baud rate: 115200, Data: 8bit, Parity: none, Stop: 1bit, Flow control: none

NOTE

- If host will use UART1, it should set WAKEUP_IN to high.

Table 3-10 List of UART1 pins

No.	Pin Name	I/O	Description
80	UART1_CTS	I	UART1 Clear to Send. 0V=not active (Data bit=0) 1.8V=active (Data bit=1)
81	UART1_RTS	O	UART1 Ready to Send. 0V=not active (Data bit=0) 1.8V=active (Data bit=1)
82	UART1_Rx	I	UART1 Receiving data. Active low 0V=active (Data bit=1) 1.8V=not active (Data bit=0)
83	UART1_Tx	O	UART1 Transmitting data. Active low 0V=active (Data bit=1) 1.8V=not active (Data bit=0)

Table 3-11 List of UART2 pins

No.	Pin Name	I/O	Description
106	UART2_Rx	I	UART2 Receiving data. 0V=active (Data bit=1) 1.8V=not active (Data bit=0)
107	UART1_Tx	O	UART2 Transmitting data. 0V=active (Data bit=1) 1.8V=not active (Data bit=0)

3.6. USIM Card Interface

3.6.1. Overview

This device supports the usage and control (including powering) of an external USIM.
The module supports Class C (1.8V).
To achieve ultra-low power consumption, SIM power will be off during Hibernation.
The USIM input/output lines are following USIM specifications.

3.6.2. Circuit Recommended for the USIM Card Interface

As the module is not equipped with an USIM card adapter, you need to place an USIM card adapter on the user interface board.

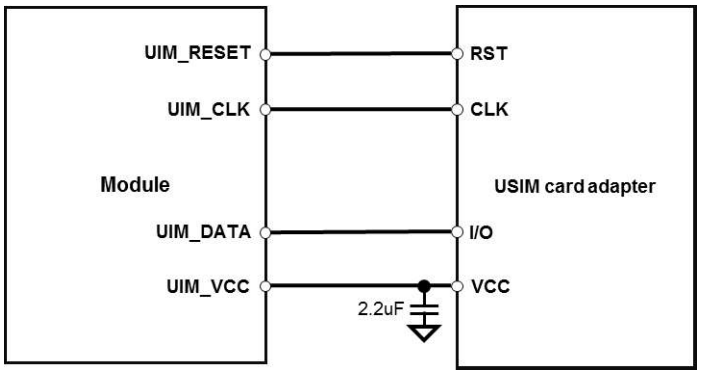


Figure 3-12 Connections of the USIM card interface

3.7. GPIO Pins

The module has some GPIO pins for connecting to external circuits.
Power supply of GPIO pin is supplied by internal circuit.

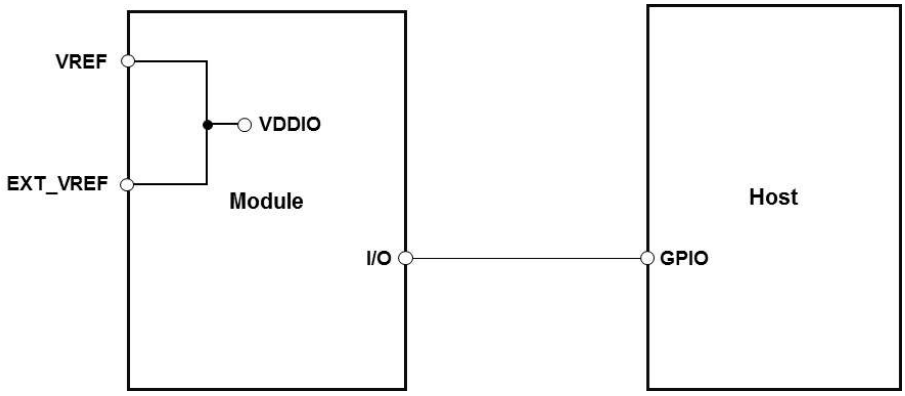


Figure 3-13 Connections of the GPIO pin

VDDIO is connected to VREF.
VREF is connected to the internal LDO of the module.
VREF is 1.8V supply voltage which is internally generated.

Table 3-12 List of GPIO pins

Pin No.	Pin Name
76, 77, 78, 79	GPIO

Table 3-13 DC Characteristics of GPIO pin

Parameter	Min.	Typ.	Max.	Unit
V_{IH}	0.85 * VDDIO	-	VDDIO + 0.3	V
V_{IL}	-0.3	-	0.25 * VDDIO	V
V_{OH}	1.6	-	VDDIO	V
V_{OL}	0	-	0.45	V
VDDIO	1.76	1.8	1.84	V

3.8. NC Pins

Table 3-14 List of NC pins

Pin No.	Pin Name	Description
3, 9, 27, 33, 43, 63, 87, 122, 142	NC	Not Connected

3.9. RF Antenna Interface

3.9.1. RF Connector location

This module does not include any antennas. External antennas need to be used for the final products using this module.

NOTE

- You should prepare an external antenna which was certified based on the Radio Type Approval of the module.
- Please optimize impedance matching between RF input/output line and antenna by using a matching circuit.
  The RF input/output line of characteristic impedance in the module is 50Ω.
- In order to diversity received, two antennas are required. (main antenna, sub antenna)
- One antenna (main antenna) can be used, but the reception sensitivity of Rx gets worse.
  If only main antenna is used, the terminal of sub antenna is terminated with 50Ω.
- Do not connect two antenna terminals together in one antenna.

4. RF Specifications

4.1. Operating Frequencies

Table 4-1 shows the RF bands supported by the module

Operating Band	Tx	Rx	Bandwidth
Band1	1940MHz－1960MHz	2130MHz－2150MHz	5MHz/ 10MHz/ 15MHz
Band19	830MHz－845MHz	875MHz－890MHz	5MHz/ 10MHz

＊For use in japan only.

4.2. Conducted RF Measurement

4.2.1. RF Test Environment

RF Test instrument	ANRITSU MT8820C
Power Divider	ANRITSU K240B
Attenuator	Keysight 8493B

NOTE

- The compensation for different frequency bands relates to the cable and the test environment.
- The instrument compensation needs to be set according to the actual cable conditions.

4.2.2. Test Standards

The module meets 3GPP TS 36.521-1 test standards. The module passes strict tests at the factory and thus the quality of the module is guaranteed.

4.3. RF Specifications

- "Test Value" in the table is the average value of the sample.
- The test values are offset in evaluation board pattern loss. Therefore, they are treated as the value of the electrode pad.
- conducted condition
- Temperature: 25 ºC

4.3.1. Rx Sensitivity

Table 4-2 Rx Sensitivity specification

Test Item		Condition	Test Value	3GPP Spec.		Unit
Band	BW		Typ.	Lower	Upper	
Band1	5MHz	FDD QPSK throughput > 95%	-106.1	-	-100	dBm
	10MHz		-103.7	-	-97	dBm
	15MHz		-101.7	-	-95.2	dBm
Band19	5MHz	FDD QPSK throughput > 95%	-106.0	-	-100	dBm
	10MHz		-103.6	-	-97	dBm

4.3.2. Tx Power

Table 4-3 UE Maximum output power

Test Item		Condition		Test Value	3GPP Spec.		Unit
Band	BW			Typ.	Lower	Upper	
Band1	5MHz	QPSK	1RB	22.4	20.3	25.7	dBm
			PRB	22.3	20.3	25.7	dBm
	10MHz		1RB	22.2	20.3	25.7	dBm
			PRB	22.1	20.3	25.7	dBm
	15MHz		1RB	22.4	20.3	25.7	dBm
			PRB	22.1	20.3	25.7	dBm
Band19	5MHz		1RB	23.5	20.3	25.7	dBm
			PRB	23.6	20.3	25.7	dBm
	10MHz		1RB	23.5	20.3	25.7	dBm
			PRB	23.5	20.3	25.7	dBm

Table 4-4 Maximum power reduction (MPR)

Test Item		Condition		Test Value	3GPP Spec.		Unit
Band	BW			Typ.	Lower	Upper	
Band1	5MHz	QPSK	PRB	22.3	20.3	25.7	dBm
			FRB	21.3	19.3	25.7	dBm
		16QAM	PRB	21.6	19.3	25.7	dBm
			FRB	20.8	18.3	25.7	dBm
	10MHz	QPSK	PRB	22.1	20.3	25.7	dBm
			FRB	21.3	19.3	25.7	dBm
		16QAM	PRB	21.7	19.3	25.7	dBm
			FRB	20.9	18.3	25.7	dBm
	15MHz	QPSK	PRB	22.1	20.3	25.7	dBm
			FRB	21.5	19.3	25.7	dBm
		16QAM	PRB	21.8	19.3	25.7	dBm
			FRB	21.0	18.3	25.7	dBm
Band19	5MHz	QPSK	PRB	23.6	20.3	25.7	dBm
			FRB	22.6	19.3	25.7	dBm
		16QAM	PRB	23.0	19.3	25.7	dBm
			FRB	22.1	18.3	25.7	dBm
	10MHz	QPSK	PRB	23.5	20.3	25.7	dBm
			FRB	22.7	19.3	25.7	dBm
		16QAM	PRB	22.9	19.3	25.7	dBm
			FRB	22.2	18.3	25.7	dBm

NOTE

- Maximum Power Reduction of LTE is according to 3GPP TS 36.521-1 as below.

Modulation	RB Allocation	Maximum Power Reduction	Unit
QPSK	≥ 1 RB, ≤ Partial RB	0	dB
	> Partial RB	≤ 1	dB
16QAM	≥ 1 RB, ≤ Partial RB	≤ 1	dB
	> Partial RB	≤ 2	dB

4.3.3. Frequency Error

Table 4-5 Frequency Error

Test Item		Condition	Test Value	3GPP Spec.		Unit
Band	BW		Typ.	Lower	Upper	
Band1	5MHz	QPSK-FRB	0.001	-0.1	0.1	ppm
	10MHz	QPSK-FRB	-0.001	-0.1	0.1	ppm
	15MHz	QPSK-FRB	0.000	-0.1	0.1	ppm
Band19	5MHz	QPSK-FRB	-0.004	-0.1	0.1	ppm
	10MHz	QPSK-FRB	-0.004	-0.1	0.1	ppm

4.3.4. EVM

Table 4-6 EVM

Test Item		Condition	Test Value	3GPP Spec.		Unit
Band	BW		Typ.	Lower	Upper	
Band1	5MHz	Max Pwr; QPSK-PRB	1.8	-	17.5	%rms
		Max Pwr; QPSK-FRB	2.1	-	17.5	%rms
		Max Pwr; 16QAM-PRB	1.8	-	12.5	%rms
		Max Pwr; 16QAM-FRB	2.1	-	12.5	%rms
	10MHz	Max Pwr; QPSK-PRB	1.7	-	17.5	%rms
		Max Pwr; QPSK-FRB	2.1	-	17.5	%rms
		Max Pwr; 16QAM-PRB	1.9	-	12.5	%rms
		Max Pwr; 16QAM-FRB	2.1	-	12.5	%rms
	15MHz	Max Pwr; QPSK-PRB	1.8	-	17.5	%rms
		Max Pwr; QPSK-FRB	2.1	-	17.5	%rms
		Max Pwr; 16QAM-PRB	1.9	-	12.5	%rms
		Max Pwr; 16QAM-FRB	2.1	-	12.5	%rms
Band19	5MHz	Max Pwr; QPSK-PRB	2.0	-	17.5	%rms
		Max Pwr; QPSK-FRB	1.6	-	17.5	%rms
		Max Pwr; 16QAM-PRB	2.3	-	12.5	%rms
		Max Pwr; 16QAM-FRB	1.9	-	12.5	%rms
	10MHz	Max Pwr; QPSK-PRB	1.7	-	17.5	%rms
		Max Pwr; QPSK-FRB	1.7	-	17.5	%rms
		Max Pwr; 16QAM-PRB	1.9	-	12.5	%rms
		Max Pwr; 16QAM-FRB	1.9	-	12.5	%rms

4.3.5. Carrier Leakage

Table 4-7 Carrier Leakage

Test Item		Condition	Test Value	3GPP Spec.		Unit
Band	BW		Typ.	Lower	Upper	
Band1	5MHz	3.2dBm, QPSK-PRB	-36.5	-	-24.2	dBc
	10MHz	3.2dBm, QPSK-PRB	-37.5	-	-24.2	dBc
	15MHz	3.2dBm, QPSK-PRB	-40.3	-	-24.2	dBc
Band19	5MHz	3.2dBm, QPSK-PRB	-37.4	-	-24.2	dBc
	10MHz	3.2dBm, QPSK-PRB	-33. 8	-	-24.2	dBc

4.3.6. Occupied Bandwidth

Table 4-8 Occupied Bandwidth

Test Item		Condition	Test Value	3GPP Spec.		Unit
Band	BW		Typ.	Lower	Upper	
Band1	5MHz	QPSK-FRB	4.5	-	5	MHz
	10MHz		8.9	-	10	MHz
	15MHz		13.4	-	15	MHz
Band19	5MHz	QPSK-FRB	4.4	-	5	MHz
	10MHz		8.9	-	10	MHz

4.3.7. Adjacent Channel power

Table 4-9 Adjacent Channel Power (Band1)

Modulation	BW	Condition	Test Value (Typ.)		3GPP Spec.		Unit
			PRB	FRB	Lower	Upper	
QPSK	5MHz	EUTRA @-5MHz	-44.5	-46.5	-	-29.2	dB
		EUTRA @5MHz	-55.3	-45.4	-	-29.2	
		UTRA @-10MHz	-63.8	-57.3	-	-35.2	
		UTRA @-5MHz	-46.7	-47.6	-	-32.2	
		UTRA @5MHz	-56.3	-46.4	-	-32.2	
		UTRA @10MHz	-61.3	-54.2	-	-35.2	
	10MHz	EUTRA @-10MHz	-47.1	-46.9	-	-29.2	dB
		EUTRA @10MHz	-54.1	-44.9	-	-29.2	
		UTRA @-12.5MHz	-59.9	-53.3	-	-35.2	
		UTRA @-7.5MHz	-47.8	-49.1	-	-32.2	
		UTRA @7.5MHz	-57.6	-47.3	-	-32.2	
		UTRA @12.5MHz	-58.4	-50.8	-	-35.2	
	15MHz	EUTRA @-15MHz	-47.4	-46.3	-	-29.2	dB
		EUTRA @15MHz	-52.3	-44.4	-	-29.2	
		UTRA @-15MHz	-57.8	-51.7	-	-35.2	
		UTRA @-10MHz	-47.6	-49.9	-	-32.2	
		UTRA @10MHz	-56.1	-47.4	-	-32.2	
		UTRA @15MHz	-57.3	-50.2	-	-35.2	
16QAM	5MHz	EUTRA @-5MHz	-44.7	-45.9	-	-29.2	dB
		EUTRA @5MHz	-55.4	-44.8	-	-29.2	
		UTRA @-10MHz	-64.1	-57.4	-	-35.2	
		UTRA @-5MHz	-46.8	-47.0	-	-32.2	
		UTRA @5MHz	-56.4	-45.8	-	-32.2	
		UTRA @10MHz	-60.9	-54.3	-	-35.2	
	10MHz	EUTRA @-10MHz	-47.0	-46.3	-	-29.2	dB
		EUTRA @10MHz	-53.8	-44.4	-	-29.2	
		UTRA @-12.5MHz	-60.0	-53.3	-	-35.2	
		UTRA @-7.5MHz	-47.7	-48.2	-	-32.2	
		UTRA @7.5MHz	-57.5	-46.5	-	-32.2	
		UTRA @12.5MHz	-58.0	-50.9	-	-35.2	
	15MHz	EUTRA @-15MHz	-47.2	-45.7	-	-29.2	dB
		EUTRA @15MHz	-51.8	-43.9	-	-29.2	

		UTRA @-15MHz	-57.8	-51.3	-	-35.2	
		UTRA @-10MHz	-47.3	-49.1	-	-32.2	
		UTRA @10MHz	-56.0	-46.8	-	-32.2	
		UTRA @15MHz	-56.4	-49.8	-	-35.2	

Table 4-10 Adjacent Channel Power (Band19)

Modulation	BW	Condition	Test Value (Typ.)		3GPP Spec.		Unit
			PRB	FRB	Lower	Upper	
QPSK	5MHz	EUTRA @-5MHz	-40.1	-44.7	-	-29.2	dB
		EUTRA @5MHz	-50.6	-41.2	-	-29.2	
		UTRA @-10MHz	-62.7	-57.7	-	-35.2	
		UTRA @-5MHz	-42.5	-45.6	-	-32.2	
		UTRA @5MHz	-51.1	-42.0	-	-32.2	
		UTRA @10MHz	-61.3	-55.4	-	-35.2	
	10MHz	EUTRA @-10MHz	-43.3	-45.9	-	-29.2	dB
		EUTRA @10MHz	-50.9	-42.2	-	-29.2	
		UTRA @-12.5MHz	-59.1	-52.1	-	-35.2	
		UTRA @-7.5MHz	-43.8	-47.9	-	-32.2	
		UTRA @7.5MHz	-55.1	-44.0	-	-32.2	
		UTRA @12.5MHz	-55.1	-49.6	-	-35.2	
16QAM	5MHz	EUTRA @-5MHz	-40.7	-43.5	-	-29.2	dB
		EUTRA @5MHz	-50.8	-40.2	-	-29.2	
		UTRA @-10MHz	-62.4	-58.4	-	-35.2	
		UTRA @-5MHz	-43.3	-44.4	-	-32.2	
		UTRA @5MHz	-51.2	-41.1	-	-32.2	
		UTRA @10MHz	-60.7	-55.9	-	-35.2	
	10MHz	EUTRA @-10MHz	-43.8	-44.7	-	-29.2	dB
		EUTRA @10MHz	-50.3	-41.3	-	-29.2	
		UTRA @-12.5MHz	-59.0	-51.9	-	-35.2	
		UTRA @-7.5MHz	-44.3	-46.3	-	-32.2	
		UTRA @7.5MHz	-54.8	-42.9	-	-32.2	
		UTRA @12.5MHz	-54.5	-49.5	-	-35.2	

5. Electrical Specifications

5.1. Absolute Maximum Ratings

WARNING

Table 5-1 lists the absolute ratings for the module. Using the module beyond these conditions may result in permanent damage to the module.

Table 5-1 Absolute maximum ratings for the module

Symbol	Parameter	Min.	Max.	Unit
VBAT_H	VBAT_H supply pin	-0.3	5.5	V
VBAT_L	VBAT_L supply pin	-0.3	6.0	V
VDDIO	Voltage on any non-power-supply pin	-0.3	3.6	V

NOTE

- Since the voltage input to VBAT_L might be input also to the DC-DC for VBAT_H, consider the absolute maximum rating of the DC-DC.

5.2. Operating Conditions

Table 5-2 Operating conditions

Parameter	Min.	Typ.	Max.	Unit	Description
Operating temperatures	-10	-	+55	ºC	The module is fully functional (*) in all the temperature range, and it fully meets the 3GPP specification
	-30	-	+70	ºC	The module is fully functional (*) in all the temperature range
Storage temperatures	-40	-	+80	ºC	-
Module Vin (VBAT_H)	3.4	3.4	4.2	V	-
Module Vin (VBAT_L)	2.3	3.0	4.2	V	-

* Functional: the module is able to make wireless telecommunication.

5.3. Conducted Electrical Measurement

5.3.1. Electrical Test Environment

Test instrument	Keysight N6705B、Keysight N6781A

5.4. Power Supply

5.4.1. Input Power Supply

Table 5-3 Requirements for input power of the module

Parameter	Min.	Max.	Ripple Max.	Unit
VBAT_L	2.3	4.2	0.1	V
VBAT_H	3.4	4.2	0.2	V

Table 5-4 Requirements for input current of the module

Power	Peak(Maximum)
VBAT_L	300mA
VBAT_H	2000mA

NOTE

- Power voltage of our evaluation board is as follows;
  VBAT_L: 3.0V, VBAT_H: 3.4V

5.4.2. Power Consumption

Module is optimized to achieve ultra-low power consumption addressing IoT market needs. Power state is supported. (See the following Table 5-5)

Table 5-5 Power state

Power state	Description	Required supplies	Wake-up options
Shutdown	Module powered off.	-	-
Hibernation	System is halted and connected to reference 32KHz clock. Most baseband circuitry is power gated and chip registers data is not retained. DRAM is in self-refresh mode. All user/host interfaces are disabled. The UE doesn't retain output IOs (unless latched externally on the board)	VBAT LDOs and VRTC should be provided. The 1160L enables VCASN, VO18R. If SIM is required to stay alive then also the VO1830 should be kept active.	WAKEUP pin or internal RTC counter.
Active	All system is wakeup.	All required power supplies are available.	-

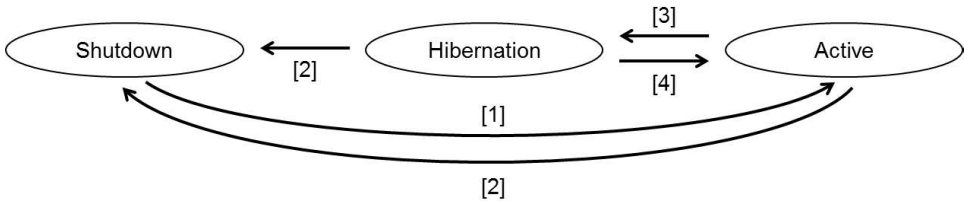


Figure 5-1 power state transition diagram

NOTE

The following part is explained of the Figure 5-1.

[1] Shutdown --> Active

See 6.1. Power on/off sequence

[2] Active or Hibernation --> Shutdown

See 6.1. Power on/off sequence

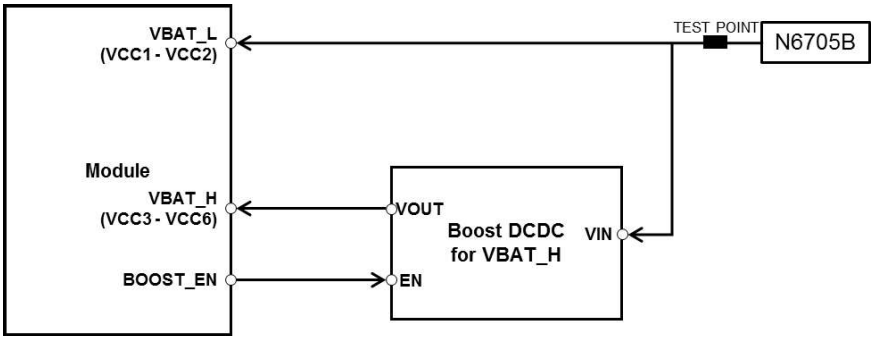
[3] Active --> Hibernation

See 6.2.3. Close data interface

[4] Hibernation --> Active

See 6.2.1. Open data interface -host to module

6.2.2. Open data interface -module to host

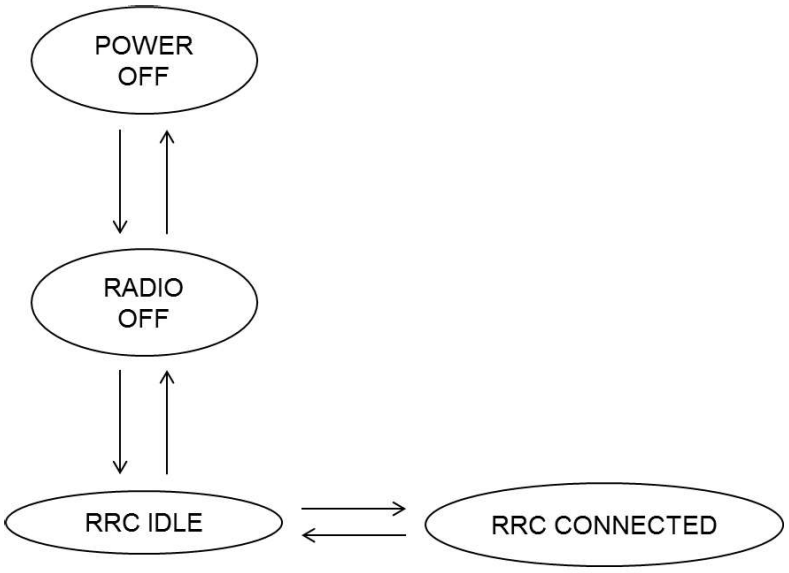


- Measured on the module at 25ºC indoor by the measuring instrument
- Band: 1, Band Width: 10MHz
- DRX cycle = 1.28s
- eDRX cycle = 81.92s, PTW = 1.28s

Table 5-6 Average power consumption of the evaluation board (3.0V)

wireless state	power state	Typical values	Notes/Condition
RRC IDLE	Hibernation	2.9mA *	DRX [1] (SIM power on) conformed to Release 10
		99uA *	eDRX [2] conformed to Release 13
RRC CONNECTED	Active	824mA *	Tx Power: 23dBm data transfer rate: 10Mbps

* All values are preliminary, subject to change.



POWER OFF : Module switched off
RADIO OFF : RF is disabled
RRC IDLE : RF is enabled
RRC CONNECTED : During transmitting and receiving data

Figure 5-2 the wireless state transition diagram

[1] image of current waveform during DRX

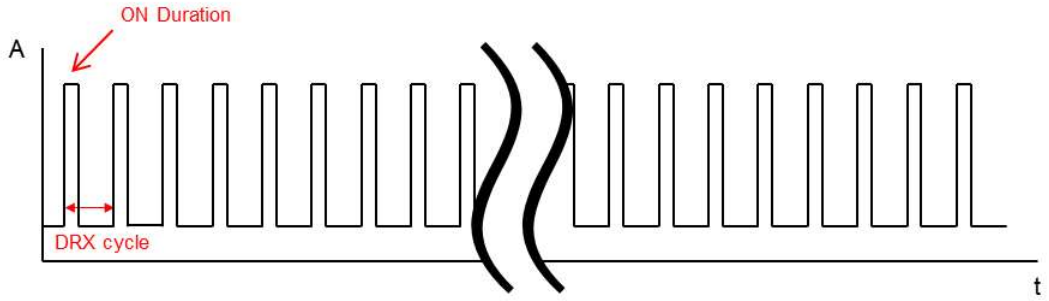


Figure 5-3 image of current waveform during DRX

[2] image of current waveform during eDRX

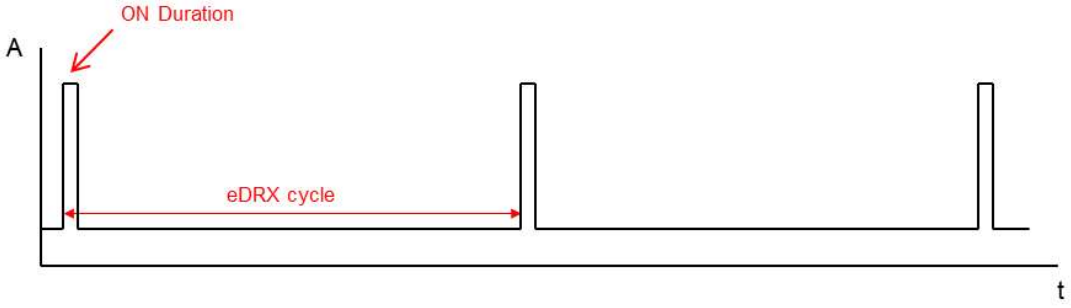


Figure 5-3 image of current waveform during eDRX

6. Function and Features

6.1. Power on/off sequence

6.1.1. Triggered by VBAT_L (VCC3 - VCC6)

The module is powered on as input triggered by VBAT_L.
When the module is powered, the RESET pin is PU internally.
HOST does not need to input a signal to the RESET pin, RESET pin should be opened.

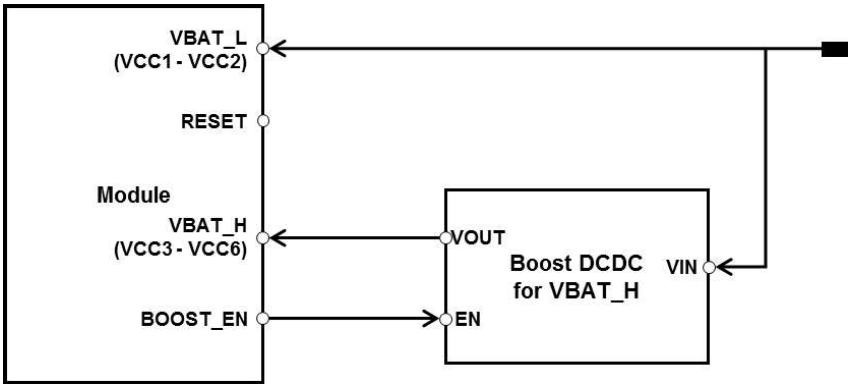


Figure 6-1 reference block diagram of power on triggered by VBAT_L

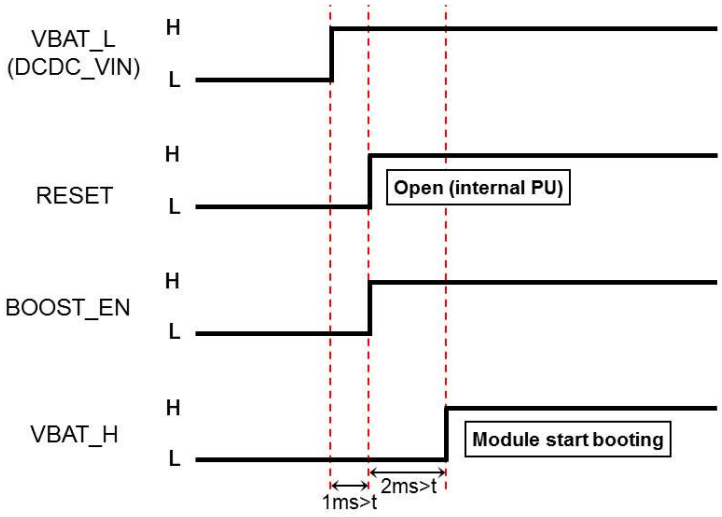


Figure 6-2 Power on sequence (triggered by VBAT_L)

VBAT_L turns off, so VBAT_H turns off. Then, module is shut down.

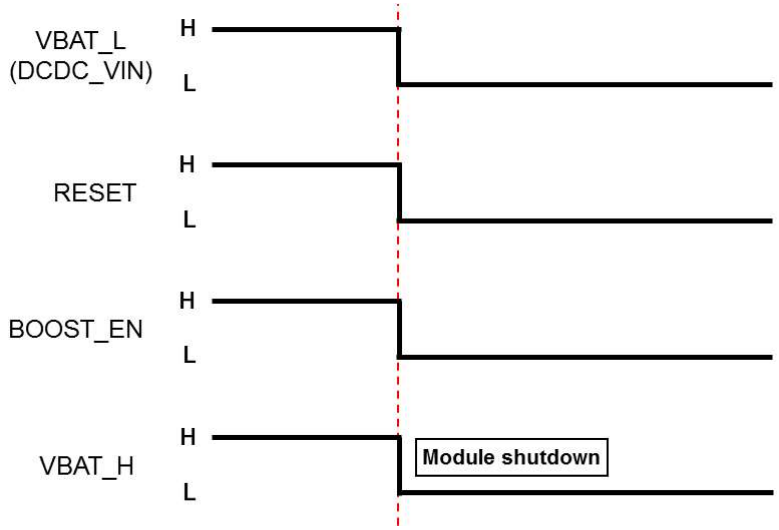


Figure 6-3 Power off sequence (triggered by VBAT_L)

NOTE

- Do not power off during module boot.
  If power off during access to flash, module may break.
- After execute software power off sequence (AT Command), you VBAT_L turn off.
  Refer to the following document for the software power off sequence.
  - Software Application Guide ("3.4. モデム機能 OFF")

6.1.2. Triggered by RESET pin

The module is powered on as input triggered by RESET pin.
MCU is powered and RESET pin is kept low.
After VBAT_H is on, release RESET pin.

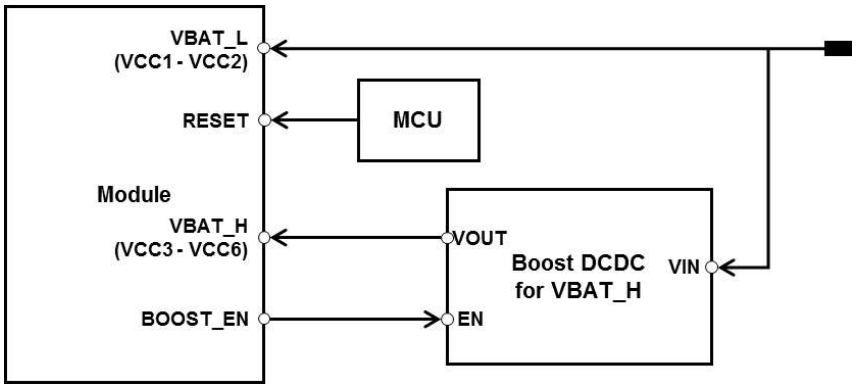


Figure 6-4 reference block diagram of power on triggered by RESET pin

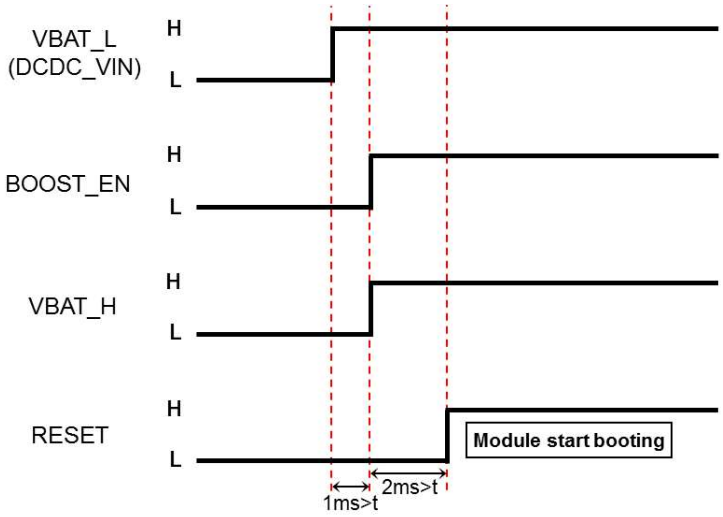


Figure 6-5 Power on sequence (triggered by RESET pin)

RESET pin is pulled low.

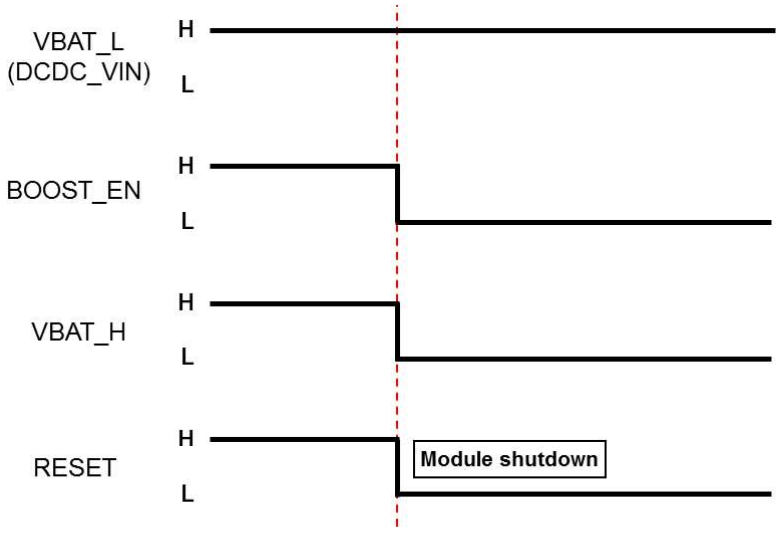
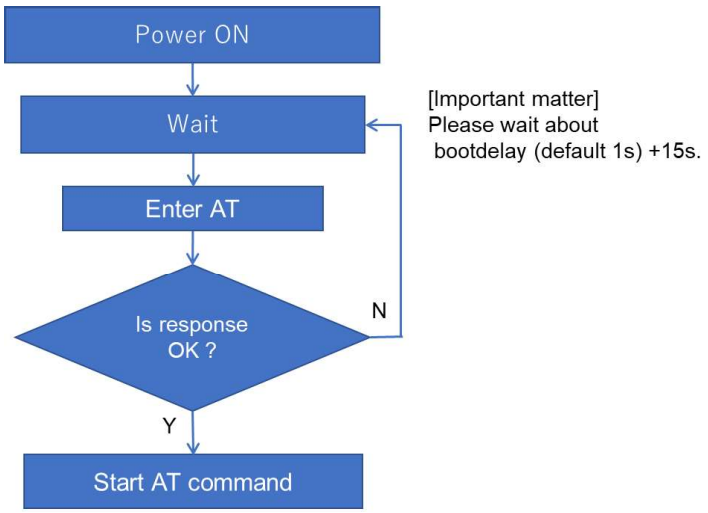


Figure 6-6 Power off sequence (triggered by RESET pin)

NOTE

- Do not power off during module boot.
  If power off during access to flash, module may break.
- After execute software power off sequence (AT Command), you VBAT_L turn off.
  Refer to the following document for the software power off sequence.
  - Software Application Guide ("3.4. モデム機能 OFF")
- A flowchart showing start AT command.



6.2. Host-Module Mutual Wakeup Interface for UART

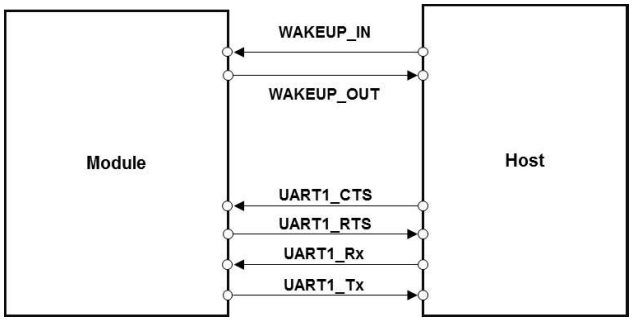


Figure 6-7 Host-Module Mutual Wakeup

The state of WAKEUP_IN and WAKEUP_OUT

(1) WAKEUP_IN (Host: Output, Module: Input)

High：When host need to open the data interface and to wake up to module.

Low：When host need to close the data interface.

(2) WAKEUP_OUT (Host: Input, Module: Output)

High：Module need to open the data interface.

Therefore, interrupt to wakeup host.

Low：Module do not need to open the data interface.

6.2.1. Open data interface –host to module

When host wants to send data to module, host should open data interface.
The timing chart is as follows. (See figure 6-8)

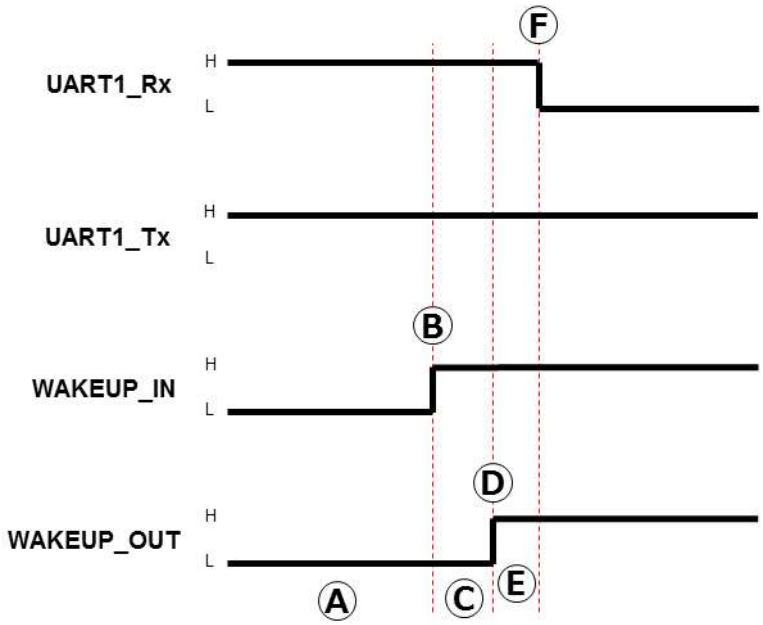


Figure 6-8 Open data interface - host to module

First, data interface state is not open
A - Host wants to send data to module
B - Host sets WAKEUP_IN to high (WAKEUP_IN = high)
C - Module is awaking (might also be waking) and module is preparing
D - Module sets WAKEUP_OUT to high (WAKEUP_OUT = high)
E - Data interface is opened and module will be able to receive data
F - Host can send data to module

NOTE

● It takes about 1ms that C is completed.
So, please host wait about 1ms between B and D.

● Host should open data interface, and send data to module. (See figure 6-8)
If data interface is not open, host should not send signal at UART1_Rx of module.
Because module sets WAKEUP_OUT to high if module receives signal at UART1_Rx.
Then state of module becomes Hibernation to Active, consumption current increase.

6.2.2. Open data interface –module to host

When module wants to send data to host, module opens data interface.

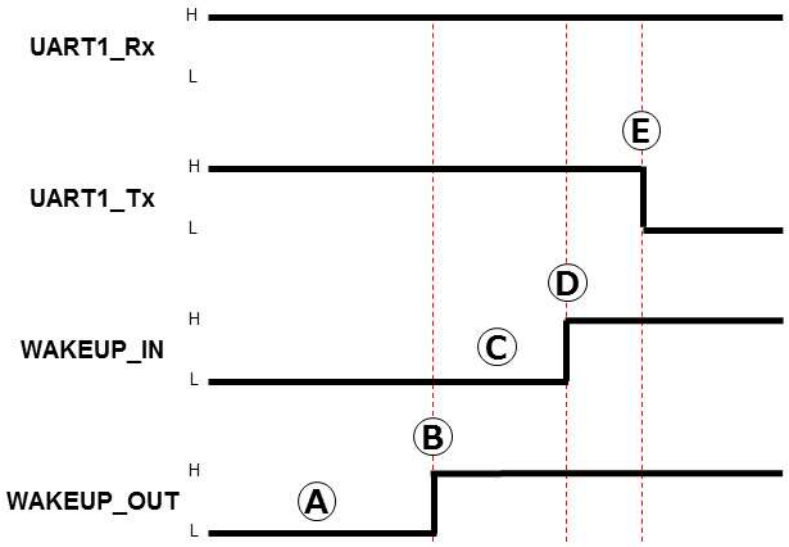


Figure 6-9 Open data interface - module to host

First, data interface state is not open.

A - Module wants to send data to host

B - Module sets WAKEUP_OUT to high (WAKEUP_OUT = high)

C - When host detects module sets WAKEUP_OUT to high, host needs to do the processing necessary to receive data

D - When host is completed the processing on UART, host sets WAKEUP_IN to high (WAKEUP_IN = high)

E - The data interface is opened and communication can start

6.2.3. Close data interface

Host has no send data and wants to close data interface.

Then shift the state of module Active to Hibernation.

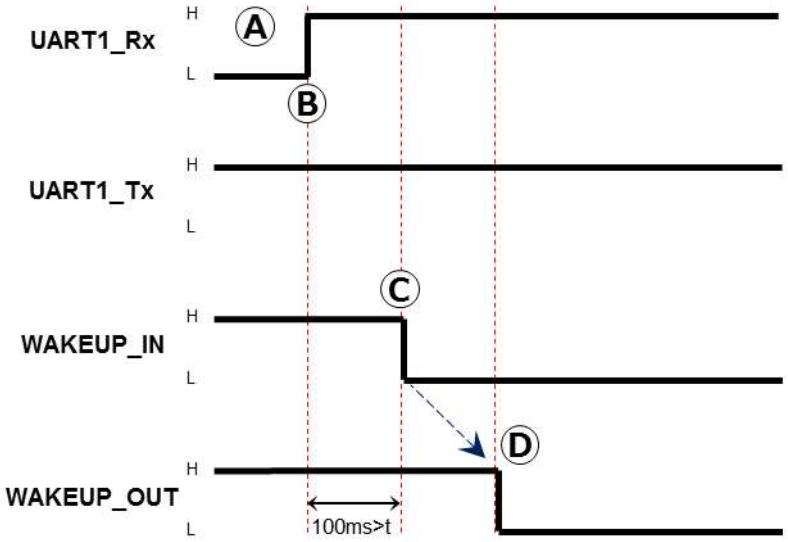


Figure 6-10 Close data interface

A - Host detects that it is sending the last data bit in a session and module is not transmitting any data (UART1_Tx=high)

B - Host will not send any data (UART1_Rx = fix=high)

C - Host sets WAKEUP_IN to low (WAKEUP_IN=low)

D - Module detects WAKEUP_IN is low, and sets WAKEUP_OUT to low (WAKEUP_OUT=low)

The point is, the data interface closes and the module will sleep

NOTE

When there are events on the LTE network, Module does not sleep. (It will not be D)

(e.g. RRC status is RRC-connected)

In that case, wait for the end of the communication event.

Since it is necessary to receive the output data of the module.

Please resume data connection.

The following figure shows the flowchart of close data interface.

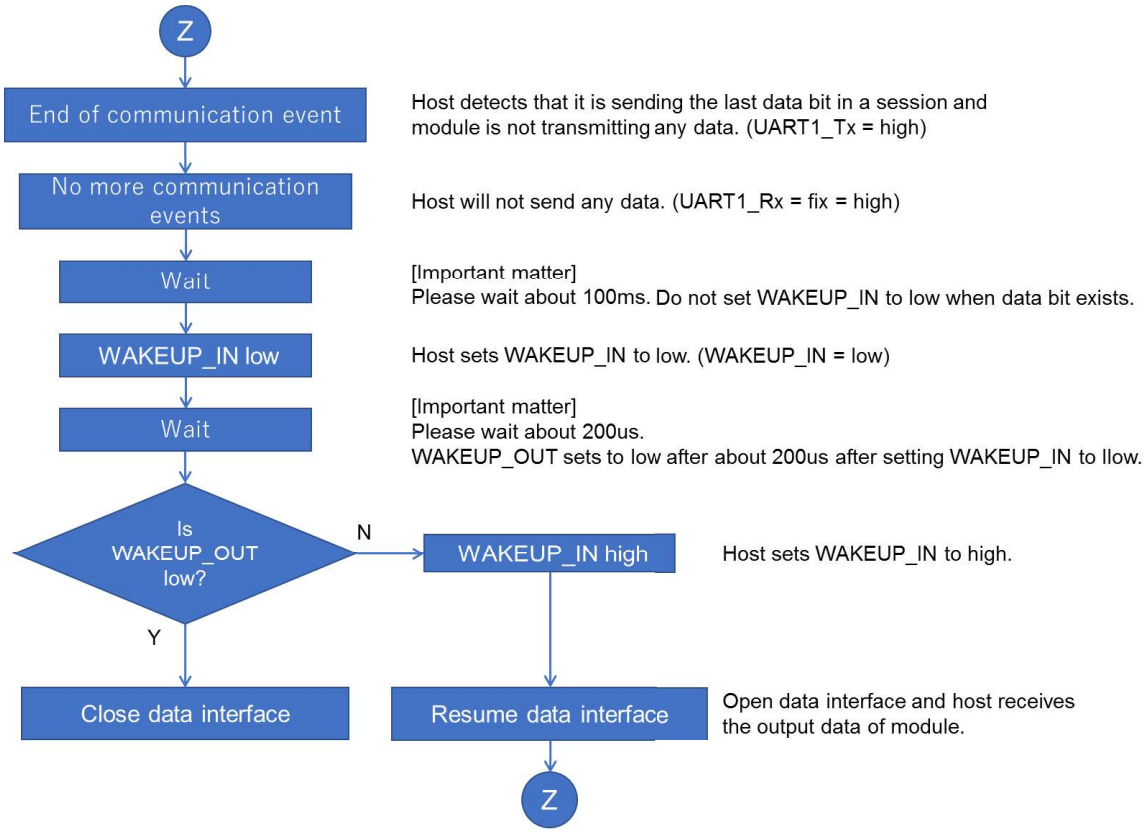


Figure 6-11 flowchart of close data interface

6.3. Detect reset of module

When module every boot, module notify "%BOOTEV:1" via UART1.
This function is default on.

6.4. Basic Reliability Features

Table 6-1 Test conditions and results of the reliability of the module

Item	Test Condition	Results
High-Temperature Storage Test	Devices are left for 2 hours in the normal temperature and humidity after being placed in a high temperature (80deg-C) environment for 100 hours, while no voltage is applied.	Devices should show no abnormal electrical performance.
Low-Temperature Storage Test	Devices are left for 2 hours in the normal temperature and humidity after being placed in a low temperature (-40deg-C) environment for 100 hours, while no voltage is applied.	Devices should show no abnormal electrical performance.
High-Temperature and Humidity Storage Test	Devices are left for 2 hours in the normal temperature and humidity after being exposed to 95% humidity at 85deg-C for 100 hours, while no voltage is applied.	Devices should show no abnormal electrical performance.
Thermal Shock Test (Air)	Devices are left for 2 hours in the normal temperature and humidity after being placed at two different temperature [-40~(transition time max.10Sec.) 85deg-C] in the atmosphere for 30 minutes respectively and this cycle is repeated 100 times.	Devices should show no abnormal electrical performance.
High Temperature Test (Biased)	After being placed in a high temperature (75deg-C) environment for 100 hours, while receiving and transmitting, the device is measured in the same environment.	Devices should show no abnormal electrical performance.
Humidity Test (Biased)	Devices are left for 2~24 hours in the normal temperature and humidity after being exposed to 95% humidity at 60deg-C for 100 hours, operating the receiver and transmitter electric circuit of devices.	Devices should show no abnormal electrical performance.
ESD (Machine Model)	C = 200pF, R = 0 ohm, +/-100V, 5 times for each terminal ESD was applied to all module terminals except GND.	Devices should show no abnormal electrical performance.
Solder Heat Resistance Test	Peak temperature 250deg-C (+5/-0deg-C), 2 times	Devices should show no abnormal electrical performance.
Vibration Test (Device)	Devices are fixed to a vibration table. overall amplitude of vibration:1.5mm at f=10~82Hz acceleration of vibration:196m/s^2 20G at f=82~2000Hz, sweep time:4 minutes (f=10~2000~10Hz) X, Y and Z-axis for 2 hours each for a total of 6 hours.	Devices should show no abnormal electrical performance.
Free Fall Test	Devices will be dropped naturally on the concrete board 6 faces*3 times at a height of 75 centimeter.	Devices should show no abnormal electrical performance.

7. Mechanical Specifications

7.1. Dimensions of the module

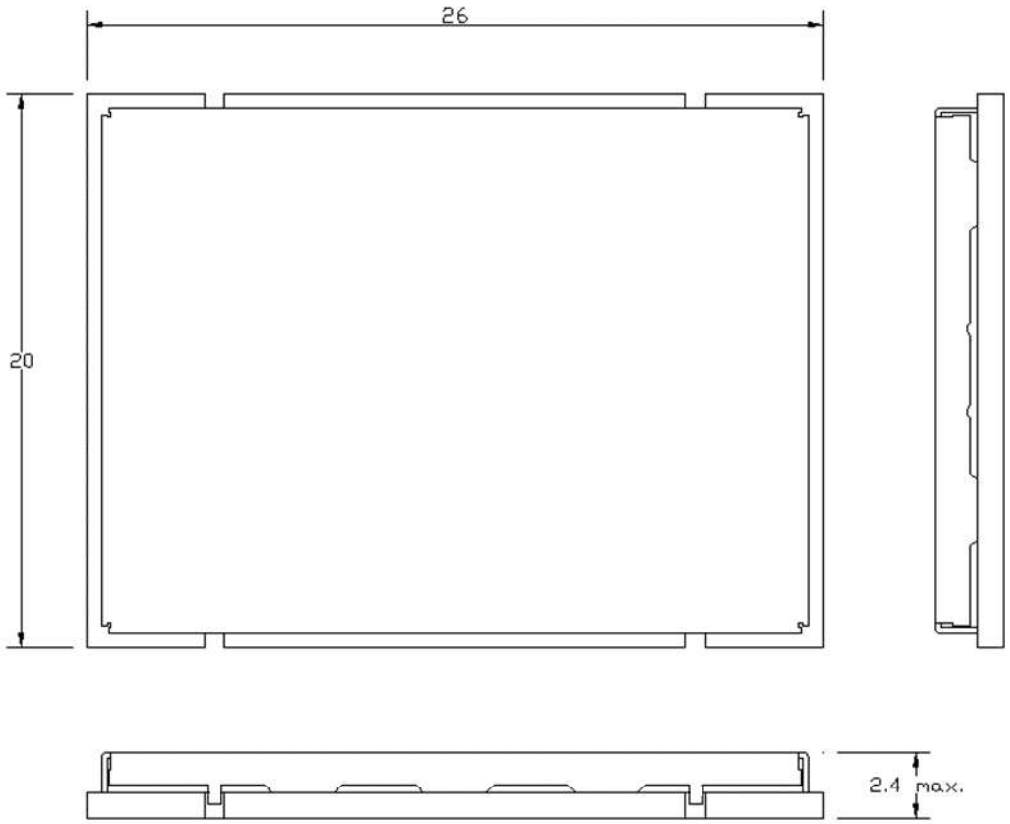


Figure 7-1 Dimensions of the module (TOP VIEW) (unit: mm)

*Tolerances unless otherwise specified: ±0.2mm

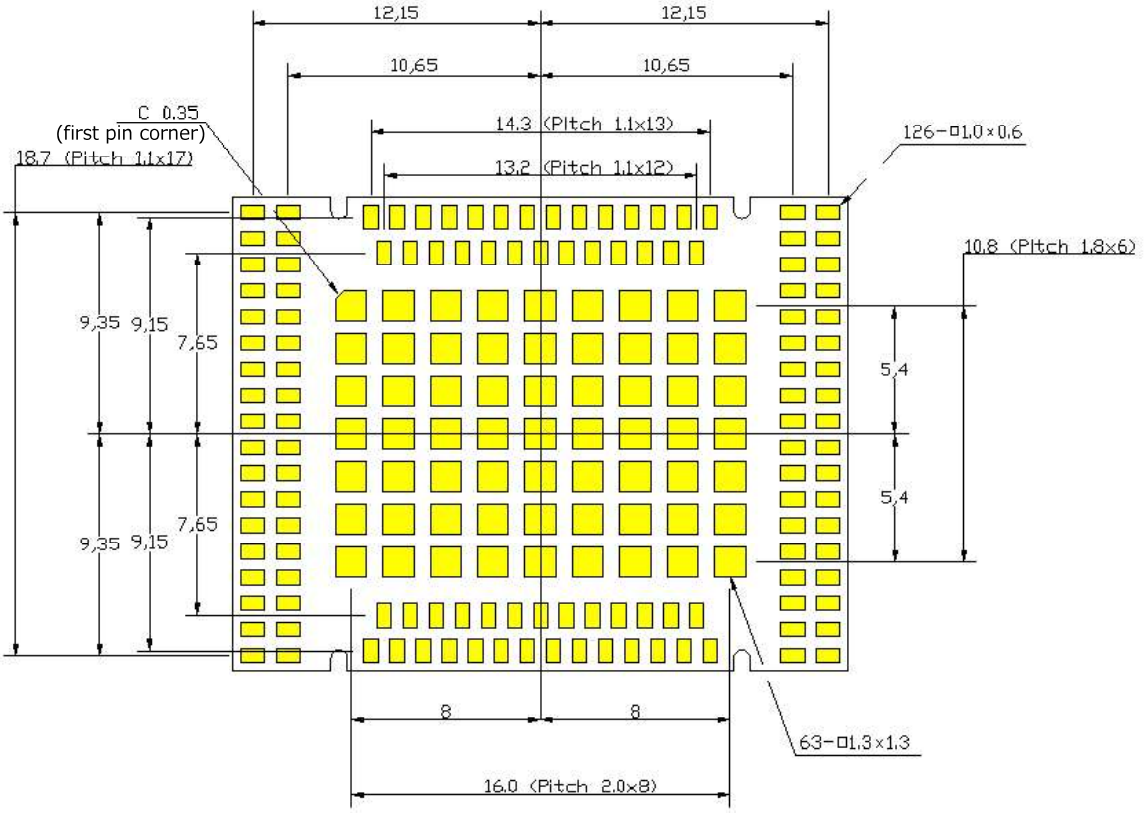
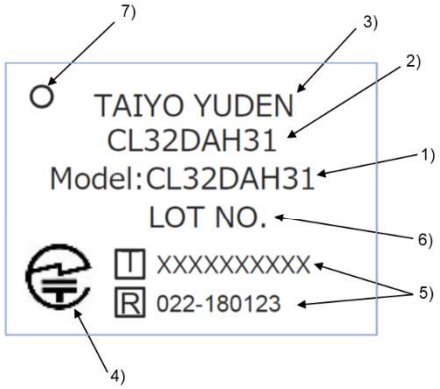


Figure 7-2 Dimensions of the module (TOP THRU VIEW) (unit: mm)

7.2. Label



1) Model : CL32DAH31
2) Part Number : CL32DAH31
3) Manufacture : TAIYO YUDEN
4) Japan logo mark: Specified logo mark
5) Japan ID : Specified ID Number
6) Lot number : Four digits
7) 1 pin mark : φ1.0mm circle mark on the shield case

Figure 7-3 Description of label

7.3. Packing System

The module package includes the tray, tray (cover), antistatic band, desiccant, and humidity indicator card.

This module is stored in the tray in units of 48 pieces.

- Packaging method: Tray
- Packaging unit: 480

  * It might be providing as tray at sample stage.

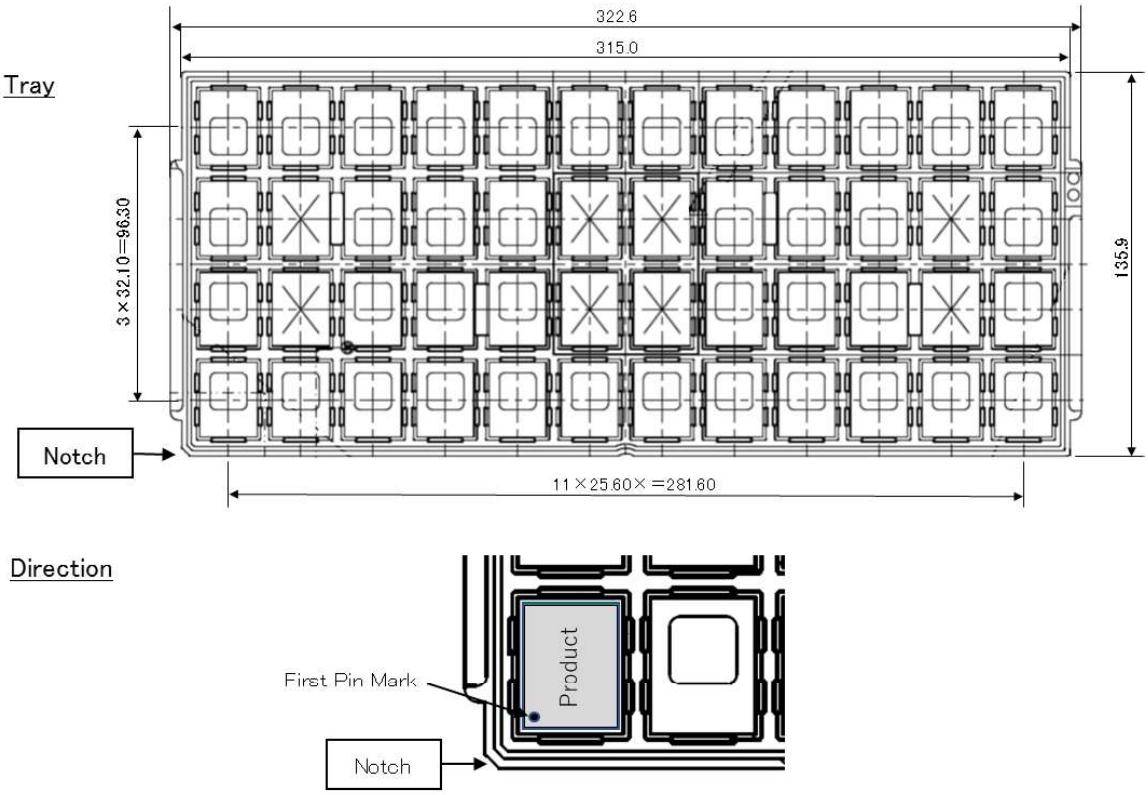


Figure 7-4 Packaging Figure

Place 10 trays, place the tray (cover) on it, and place it in an aluminum moisture barrier bag together with desiccant and humidity indicator card.
Both ends of the aluminum moisture barrier bags are sandwiched by buffer corrugated paper and placed in the inner box.
The interior box is packed in an exterior box and shipped.

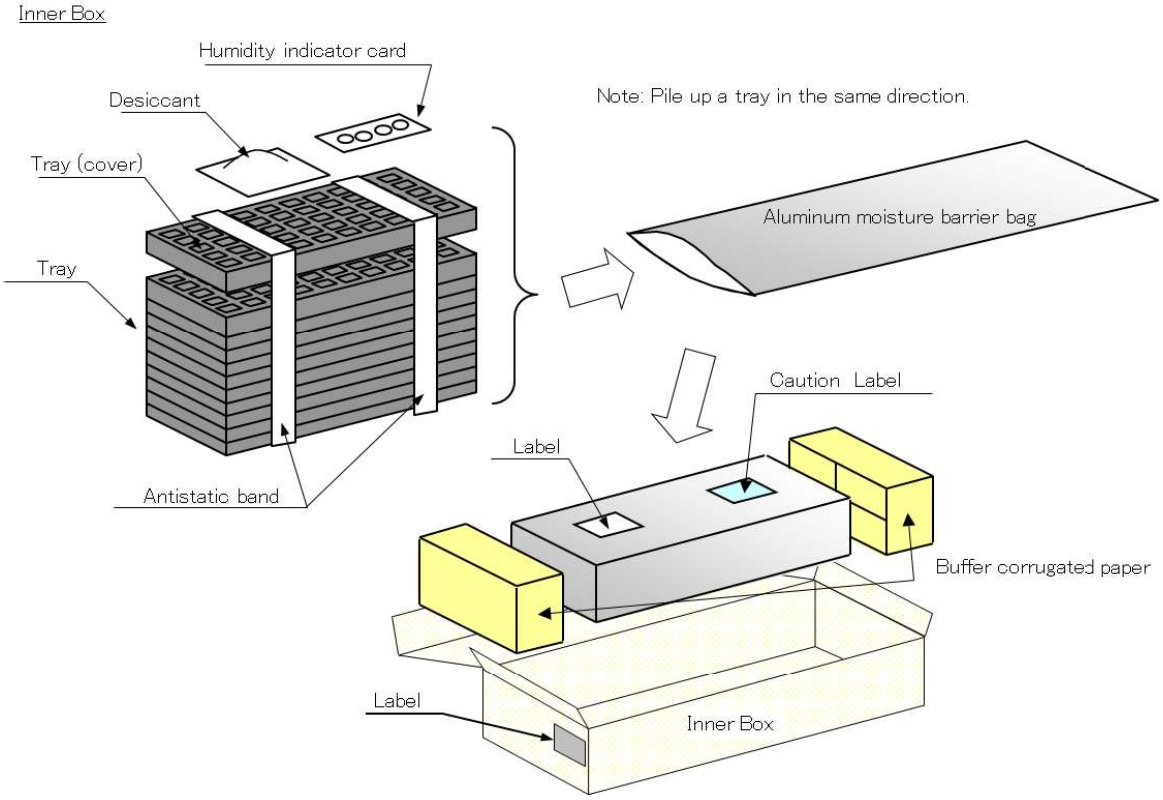


Figure 7-5 Package assembly

8. Handling Precaution

8.1. Thermal Management

CL32DAH31 have high power consumption and due to their very small size, need to be designed properly for heat dissipation.

8.2. Desire and Conditions

This specification describes desire and conditions especially for mounting.

8.2.1. Environment conditions for use and storage

1. Store the components in an environment of < 40°C /90%RH if they are in a moisture barrier bag packed by TAIYO YUDEN.
2. Keep the factory ambient conditions at < 30°C /60%RH .
3. Store the components in an environment of < 25±5°C /10%RH after the bag is opened. (The condition is also applied to a stay in the manufacture process).

8.2.2. Conditions for handling of products

Make sure all of the moisture barrier bags have no holes, cracks or damages at receiving. If an abnormality is found on the bag, its moisture level must be checked in accordance with 2 of 8.2.2.

Refer to the label on the bag.

1. All of the surface mounting process (reflow process) must be completed in 12 months from the bag sea date.
2. Make sure humidity in the bag is less than 10%RH immediately after open, using a humidity indicator card sealed with the components.
3. All of the surface mounting process (reflow process including rework process) must be completed in 168 hours after the bag is opened (inclusive of any other processes).
4. If any conditions in 8.2.1. or condition 2 and 3 of 8.2.2. are not met, bake the components in accordance with the conditions at 125°C 24h.
5. As a rule, baking the components in accordance with conditions 4 of 8.2.2. shall be once.
6. Since semi-conductors are inside of the components, they must be free from static electricity while handled. (<100V) Use ESD protective floor mats, wrist straps, ESD protective footwear, air ionizers etc., if necessary.
7. Please make sure that there are lessen mechanical vibration and shock for this module, and do not drop it.
8. Please recognize pads of back side at surface mount.
9. This module should not be cleaned.
10. Please perform temperature conditions of module at reflow within the limits of the

following.

Please give the number of times of reflow as a maximum of 2 times.

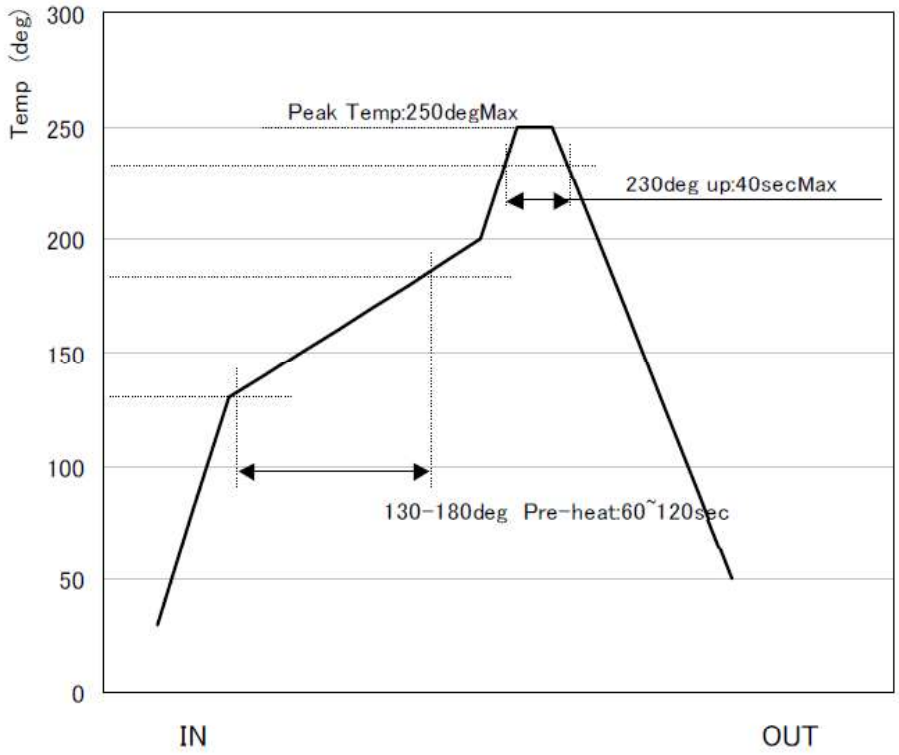


Figure 8-1 temperature conditions of module at reflow

9. Certifications

9.1. Certifications

NOTE

●Table 9-1 shows the certificate obtained by the module.

Table 9-1 Product certifications

Certification	Model Name
	CL32DAH31
technical regulations conformity certification of the Radio law	✔
Japan Approvals institute for Telecommunications Equipment	✔
Carrier IOT (docomo)	✔

10. Safety Information

Read the safety information carefully to ensure the correct and safe use of module.
Applicable safety information must be observed.

10.1. Interference

Communication between this product and other might not be established nor maintained depending upon radio environment or operating condition of this product and other products with wireless technology.
This product operates in the licensed band at 2GHz/800MHz. In case this product is used around the other wireless devices which operate in same frequency band of this product, there is a possibility that interference occurs between this product and such other devices. If such interference occurs, please stop the operation of other devices or relocate this product before using this product or do not use this product around the other wireless devices.
Power off module if using the device is prohibited. Do not use the module when it causes danger or interference with electric devices.

10.2. Medical Device

- Power off module and follow the rules and regulations set forth by the hospitals and health care facilities.
- Some module may affect the performance of the hearing aids. For any such problems, consult your service provider.
- Pacemaker manufacturers recommend that a minimum distance of 15 cm be maintained between the module and a pacemaker to prevent potential interference with the pacemaker. If you are using an electronic medical device, consult the doctor or device manufacturer to confirm whether the radio wave affects the operation of this module.

10.3. Area with Inflammables and Explosives

To prevent explosions and fires in areas that are stored with inflammable and explosive devices, power off module and observe the rules. Areas stored with inflammables and explosives include but are not limited to the following:

- Gas station
- Fuel depot (such as the bunk below the deck of a ship)
- Container/Vehicle for storing or transporting fuels or chemical products
- Area where the air contains chemical substances and particles (such as granule, dust, or metal powder)
- Area indicated with the "Explosives" sign
- Area indicated with the "Power off bi-direction wireless equipment" sign
- Area where you are generally suggested to stop the engine of a vehicle

10.4. Airline Security

Observe the rules and regulations of airline companies. When boarding or approaching a plane, power off module. Otherwise, the radio signal of the module may interfere with the plane control signals.

10.5. Safety of Children

Do not allow children to use the module without guidance. Small and sharp components of the module may cause danger to children or cause suffocation if children swallow the components.

10.6. Environment Protection

Observe the local regulations regarding the disposal of your packaging materials, used module, and promote their recycling.

10.7. RoHS Approval

The module is in compliance with the restriction of the use of certain hazardous substances in electrical and electronic equipment Directive 2011/65/EU (RoHS Directive).

10.8. Laws and Regulations Observance

Observe laws and regulations when using module. Respect the privacy and legal rights of the others.

10.9. Care and Maintenance

It is normal that module gets hot when you use or charge it. Before you clean or maintain the module, stop all applications and power off the module.

- Use module with care and in clean environment. Keep the module from a fire or a lit cigarette.
- Protect module from water and vapor and keep it dry.
- Do not drop, throw or bend module.
- Clean module with a piece of damp and soft antistatic cloth. Do not use any chemical agents (such as alcohol and benzene), chemical detergent, or powder to clean it.
- Do not leave module in a place with a considerably low or high temperature.
- Do not dismantle the module. Otherwise, the module is not covered by the warranty.

10.10. Emergency Call

This module functions through receiving and transmitting radio signals.
Therefore, the connection cannot be guaranteed in all conditions. In an emergency, module cannot be used.

11. Appendix Acronyms and Abbreviations

Term	Definition
ADC	Analog-to-Digital Converter
AFE	Analog Front End
BSP	Board Support Package
DAC	Digital-to-Analog Converter
DC	Direct Current
DRX	Discontinuous Reception
eDRX	Extended DRX
EJTAG	Embedded Joint Test Action Group
ESD	Electro-Static Discharge
EU	European Union
EUTRA	Evolved Universal Terrestrial Radio Access
FDD	Frequency Division Duplex
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
IMS	IP Multimedia Subsystem
I2S	Inter-IC Sound
JTAG	Joint Test Action Group
LGA	Land Grid Array
LPDDR	Low Power DDR
LTE	Long Term Evolution
MCP	Multi-chip Package
MCU	Micro Controller Unit
MISO	Multiple In Single Out
NC	Not Connected
OFDM	Orthogonal Frequency Division Multiplexing
OFDMA	Orthogonal Frequency Division Multiple Access
OMADM	Open Mobile Alliance-Device Management
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PMU	Power Management Unit
PTW	Paging Time Window
PWM	Pulse Width Modulation
QAM	Quadrature Amplitude Modulation

QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RoHS	Restriction of the Use of Certain Hazardous Substances
RRC	Radio Resource Control
RTC	Real Time Clock
Rx	Receive
SC-FDMA	Single-Carrier Frequency Division Multiple Access
SDR	Software Defined Radio
SMS	Short Message Service
SPI	Serial Peripheral Interface
SUPL	Secure User. Plane Location
TCXO	Temperature Compensated Crystal Oscillator
Tx	Transmit
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module
UTRA	Universal Terrestrial Radio Access
VoLTE	Voice over LTE
XO	Crystal Oscillator. Typically used to indicate a Crystal connection to the IC (utilizing internal Oscillator)