LTE Cat-M1

Multi Band Module

WSCLxADAH2Z
Datasheet

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Application

Restricted to M2M Device. *Not allowed for TELEMATICS use cases.

"M2M Device" hereinto is defined as a complete device that connects to network infrastructure equipment over a wireless network utilizing Wireless Wide-Area Network Standard through the module; utility metering devices, vending machines, cargo containers, ATM machines for electronic payment, remote monitoring systems, digital billboards, portable healthcare monitoring devices, alarm or security systems, portable tracking devices. Telephones and tablet devices are not included in the "M2M Devices".

● Revision History

Revision	Date	Summary of Change
1.0	2023.09.29	-

● Contents

● Relation Documents

- Software Application Guide
- Hardware Application Guide
- AT Commands Manual
- Circuit of EVB (recommended circuit)
- Evaluation Board Manual

1. Introduction

TAIYO YUDEN offers a turnkey solution of Cat-M1 multi band LGA module supporting the following key features:

Module highlights

- Based on Altair Semiconductor ALT1250 chipset
- LTE Cat-M1
- Supporting standard multi band design
  - 1 x Band1 (2GHz)
  - 1 x Band19 (800MHz)
  - 1 x Band26 (800MHz)
- Small size (module size 15.0mm x 14.0 mm x 1.9 mm)
- Power supply: 2.3-4.35V (VBAT / VBAT_FEM)
- Supports ultra-low DRX, eDRX, PSM and standby power consumption

LTE features highlights

- LTE Cat-M1 support based on 3GPP release13
- SW upgradable to Cat-M1 based Release14

Features

- LwM2M, TCP/IP, UDP/IP, SMS, Power saving

Interface support

- UART

Model name

W S　C L x A D A H 2 Z
①　②　③④　⑤　⑥⑦

①	merchandise category (商品区分)	WS	：Product code (商品コード)
②	Module identification (モジュール識別)	CL	：Cellar LTE
③	Band (使用バンド)	2	：Band26、 3 ：Band1,Band19
④	Chip category (チップカテゴリ)	A	：Cat.M1
⑤	Hard configuration (ハード構成)	DAH	：LGA、ALTAIR chip
⑥	Power supply configuration (電源構成)	2	：2 power supply (2電源)
⑦	Memory capacity (メモリ容量)	Z	：128Mbit

This document describes the hardware application interfaces and air interfaces that are provided when the module is used.
This document helps you to understand the interface specifications, electrical features and related product information of the module.

2. Overall Description

2.1. Function Overview

Table1 Features

Feature	Description
Physical Features	Dimensions:15.0mm × 14.0mm × 1.9mm
Weight	0.92g
Operating Band	Band1, 19, 26
Operating Temperature [1]	–30 to +70°C
Storage Temperature	–40 to +80°C
Power Voltage	VBAT: 2.3V to 4.2V [2] VBAT_FEM: 2.85V to 4.5V [2]
Application Interface	Serial communication interface UART0 (for AT) UART1 (for debug [3]) UART2 (for CLI (FW update etc.) [3])
	Control signal SC_SWP, PMU_SHUTDOWN, PMU_WAKEUP, AUX_ADC4 (BOOST_EN)
	USIM Card Interface
SMS	Supports formats of PDU (AT command) SMS over SGs
Data Services	Half-Duplex DL: 300kbps (OFDMA) / UL: 375kbps (SC-FDMA) [4]
Operating System	Real Time OS

[1]: 3GPP release 13 compliant

[2]: Power voltage of our evaluation board is as follows; VBAT: 3.0 V
VBAT_FEM: 3.3 V

[3]: UART1 and UART2 is used for debug and FW update. So, please prepare test pads for external connection.

[4]: the maximum value in theory

2.2. Circuit Block Diagram

Figure1 shows the circuit block diagram of the module. The application block diagram and major functional units of the module contain the following parts:

- Radio Frequency (RF) transceiver + BaseBand (BB) unit
- Multi-chip package (MCP) include Power Management Unit (PMU)
- RF Front End Module (FEM)

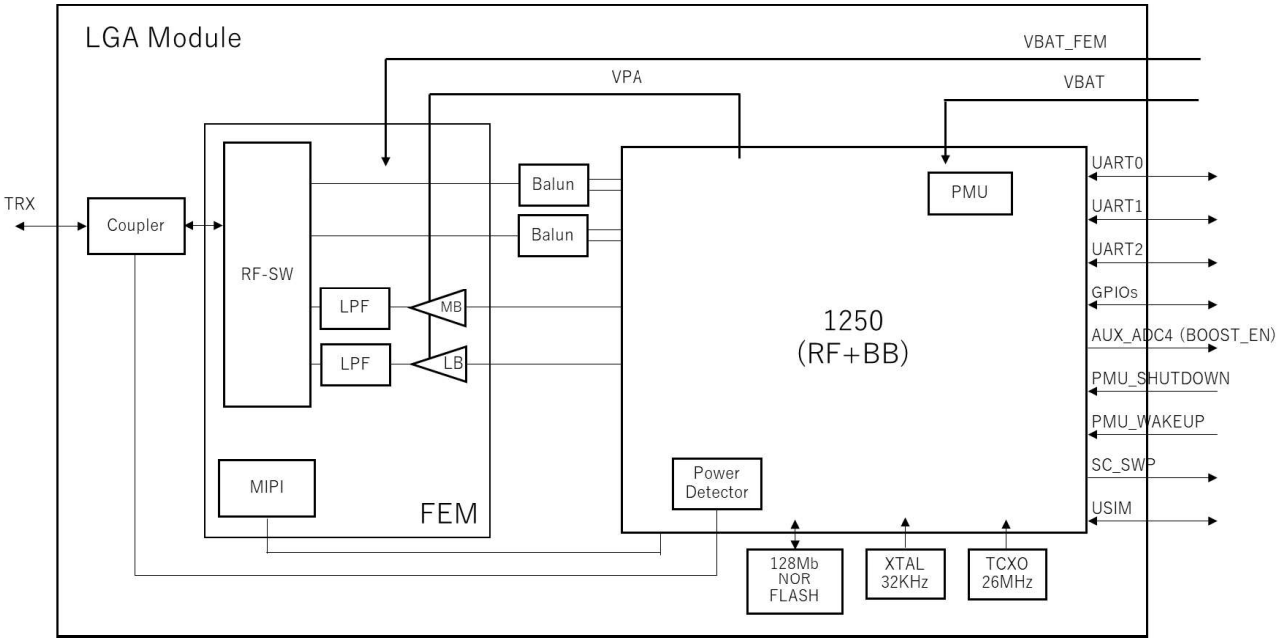


Figure1 circuit block diagram of the module

3. Description of the Application Interfaces

3.1. pin

The module uses pins as its external interfaces.
Figure2 shows an LGA map diagram of this module. Table2 shows definitions of pins on the LGA map.

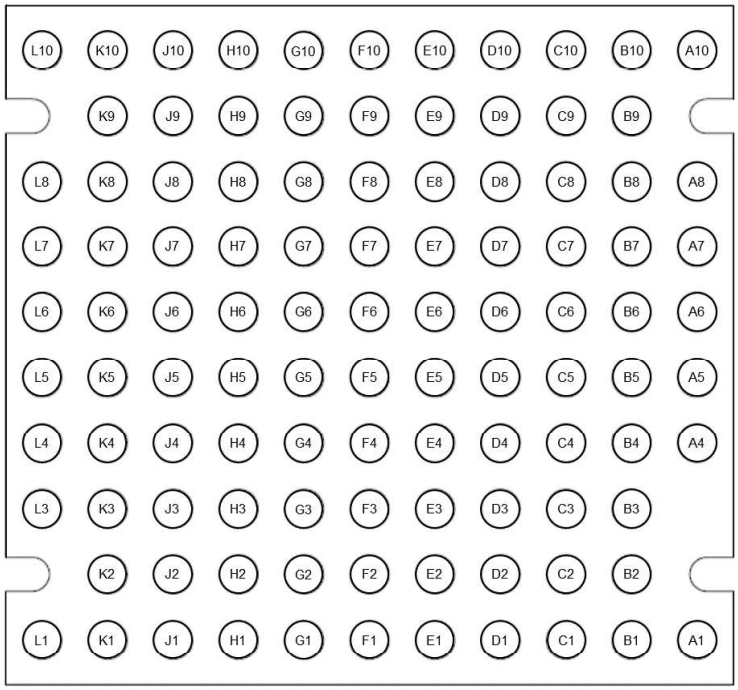


Figure2 LGA map diagram (TOP_THRU_ VIEW)

Table2 Definitions of pins

No.	Pin Name	Direction	Type	Reset Value	Recommendation for Unused pin	Description
A1	GND	-	-	-	-	Ground
A4	GND	-	-	-	-	Ground
A5	RF_AUX_OUT1	-	A	-	Open	Reserved
A6	GND	-	-	-	-	Ground
A7	RF_RXTX	IO	A	-	-	RF TXRX Main LTE antenna
A8	GND	-	-	-	-	Ground
A10	GND	-	-	-	-	Ground
B1	VBAT_FEM	I	P	-	-	Module input power supply
B2	VBAT_FEM	I	P	-	-	Module input power supply
B3	VBAT_FEM	I	P	-	-	Module input power supply
B4	GND	-	-	-	-	Ground
B5	GND	-	-	-	-	Ground
B6	GND	-	-	-	-	Ground
B7	GND	-	-	-	-	Ground
B8	GND	-	-	-	-	Ground
B9	UART2_RX	I	D	PU	Open	UART2 receiving data
B10	UART2_RTS	O	D	PU	Open	UART2 request to send
C1	GND	-	-	-	-	Ground
C2	GND	-	-	-	-	Ground
C3	GND	-	-	-	-	Ground
C4	GND	-	-	-	-	Ground
C5	GND	-	-	-	-	Ground
C6	VDD_RF	O	P	-	Open	VDD_RF out
C7	GND	-	-	-	-	Ground
C8	UART0_RX	I	D	PU	Open	UART0 receiving data
C9	UART2_TX	O	D	PU	-	UART2 transmitting data
C10	UART2_CTS	I	D	PD	Open	UART2 clear to send
D1	EJ_TRST	IO	D	PD	Pull down (10kΩ)	Reserved
D2	I2C0_SCL	IO	D	PU	Open	Reserved
D3	I2C0_SDA	IO	D	PU	Open	Reserved
D4	PMU_EXT_ALARM	O	A	-	Open	Module's power mode 'High' is active state, 'Low' is inactive state
D5	FE_DEBUG	-	-	-	-	Ground
D6	GND	-	-	-	-	Ground

No.	Pin Name	Direction	Type	Reset Value	Recommendation for Unused pin	Description
D7	GND	-	-	-	-	Ground
D8	UART0_TX	O	D	PU	-	UART0 transmitting data
D9	UART0_CTS	I	D	PU	Open	UART0 clear to send If this pin is connected to open drain output of host, pull up this pin to VDDIO_GPM via not more than 10K ohm register
D10	VDD_XO	O	P	-	Open	VDD_XO out
E1	EJ_TDO	IO	D	PU	Open	Reserved
E2	EJ_TDI	IO	D	PD	Open	Reserved
E3	SC_SWP	O	D	PD	Open	Host wakeup
E4	PMU_POWER_BUTTON	I	A	-	PU*	Reserved *It is PU (min:600kΩ). Pull source is VRTC.
E5	DCDC_1v3	O	P	-	Open	DCDC_1v3 out
E6	GND	-	-	-	-	Ground
E7	GND	-	-	-	-	Ground
E8	UART0_RTS	O	D	PU	Open	UART0 request to send
E9	GND	-	-	-	-	Ground
E10	RESERVED0_USB_DN	-	-	-	Open	Reserved
F1	EJ_TCK	IO	D	PD	Open	Reserved
F2	EJ_TMS	IO	D	PD	Open	Reserved
F3	VDD_DIG	O	P	-	Open	VDD_DIG out
F4	DEBUG_SEL	IO	D	PD	Open	Reserved
F5	TEST	-	-	-	-	Ground
F6	GND	-	-	-	-	Ground
F7	GND	-	-	-	-	Ground
F8	AUX_ADC4 (BOOST_EN)	O	D	PD	Open	1.8V = enable the external DC-DC for VBAT_FEM power
F9	RESERVED2_USB3V	-	-	-	Open	Reserved
F10	RESERVED0_USB_DP	-	-	-	Open	Reserved
G1	GND	-	-	-	-	Ground
G2	PMU_SHUTDOWN	I	A	-	PU*	Shutdown active low. HW reset. *It is PU (min:600kΩ). Pull source is VRTC.
G3	PMU_ATB	I	-	-	Open	Reserved
G4	PMU_WAKEUP	I	A	-	PD (10KΩ)	Device wakeup, active high

No.	Pin Name	Direction	Type	Reset Value	Recommendation for Unused pin	Description
G5	DEBUG_RSTN	IO	D	PU	Open	Reserved
G6	UART1_RTS	O	D	PU	Open	UART1 request to send
G7	GND	-	-	-	-	Ground
G8	SF_nHOLD/IO3	IO	D	-	Open	Reserved
G9	SPIM0_EN1	IO	D	PU	Open	Reserved
G10	VFLASH	O	P	-	Open	VFLASH out
H1	VBAT	I	P	-	-	Module input power supply
H2	VDD_EXTRA	O	P	-	Open	VDD_EXTRA out
H3	PMU_AT_OUT	O	A	-	Open	Reserved
H4	PMU_VCAP	O	A	-	Open	Reserved
H5	VDD_GPM	O	P	-	Open	VDD_GPM out
H6	SPIM1_CLK	IO	D	PD	Open	Module's reset indicator "High" is resetting.
H7	SPIM1_MISO	IO	D	PD	Open	Reserved
H8	GND	-	-	-	-	Ground
H9	UART1_TX	O	D	PU	Open	UART1 transmitting data
H10	GND	-	-	-	-	Ground
J1	VBAT	I	P	-	-	Module input power supply
J2	SIM_DETECT	I	D	PD	Open	SIM detection If use eSIM, it is NC. 0V=Unimplemented 1.8V=SIM detect
J3	PMU_AT_IN	I	A	-	-	Ground
J4	PMU_VBACKUP	I	-	-	Connect to VBAT	Reserved
J5	CLKOUT	O	D	PU	Open	Reserved
J6	SPIM1_EN	IO	D	PU	Open	Reserved
J7	SPIM1_MOSI	IO	D	PD	Open	Reserved
J8	GND	-	-	-	-	Ground
J9	GND	-	-	-	-	Ground
J10	UART1_RX	I	D	PU	Open	UART1 receiving data
K1	GND	-	-	-	-	Ground
K2	SIMIO	IO	D	PD	-	SIM data
K3	SIMRST	O	D	PD	-	SIM reset
K4	PMU_VRTC	O	P	-	Open	Used for PMU_SHUTDOWN and PMU_POWER_BUTTON pull source
K5	VDDIO_GPM	O	P	-	Open	VDDIO_GPM out
K6	GND	-	-	-	-	Ground

No.	Pin Name	Direction	Type	Reset Value	Recommendation for Unused pin	Description
K7	GND	-	-	-	-	Ground
K8	GND	-	-	-	-	Ground
K9	GND	-	-	-	-	Ground
K10	UART1_CTS	I	D	PU	Open	UART1 clear to send
L1	GND	-	-	-	-	Ground
L3	SIMCLK	O	D	PD	-	SIM clock
L4	VSIM	O	P	-	-	VSIM out The external capacitor is max 1uF.
L5	SF_nWP/IO2	IO	D	-	Open	Reserved
L6	SF_SO/IO1	IO	D	-	Open	Reserved
L7	SF_CLK	O	D	-	Open	Reserved
L8	SF_SI/IO0	IO	D	-	Open	Reserved
L10	GND	-	-	-	-	Ground

NOTE

- **I:** Input only functionality. **O:** Output only functionality.
  IO: Both input and output functionality.
- **A**: Analog pin. **D**: Digital pin. **PD**: Pull Down. **PU**: Pull Up. **P**: Power
- **Reserved**: Unused pin. Do not connect to external equipment.
- The internal resistance of digital pin is 13kΩ to 45kΩ.

3.1.1. Default Pin Allocation for Hosted Applications

Figure3 shows the recommended connections for external devices.

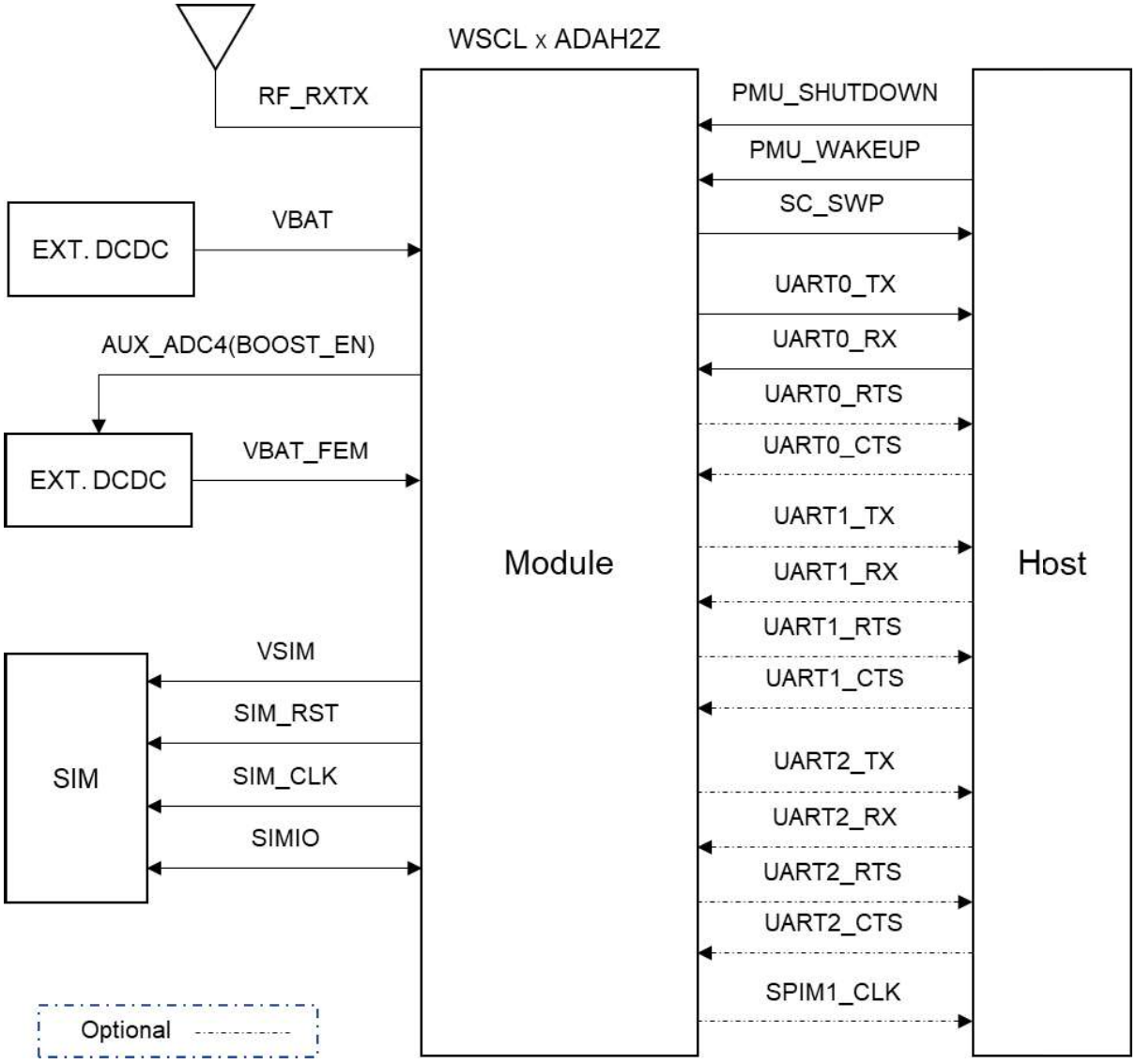


Figure3 Recommended Connections for External Devices

3.2. Power Supply Interface

3.2.1. Overview

The ALT1250 includes an integrated PMU. The PMU is designed to work directly from both rechargeable and primary batteries. The PMU supplies current to all ALT1250 blocks, the IOs, the External Flash, the TCXO and the UICC.
In addition, the PMU includes a low power RTC.
The power supply part of the module contains:

- RTC (Real Time Clock)
- APC (Advance Power Controller)
- Different regulators (LDOs and DC-DC)

Refer to Hardware Application Guide (Power supply design) for details.

Table3 lists the definitions of the pins on the power supply interface

Pin No.	Signal Name	I/O	Description	voltage (V)
B1	VBAT_FEM	I	Module input power supply	2.3-4.35
B2	VBAT_FEM	I		
B3	VBAT_FEM	I		
H1	VBAT	I	Module input power supply	2.3-4.35
J1	VBAT	I		
C6	VDD_RF	O	VDD_RF out	1.9
D10	VDD_XO	O	VDD_XO out	1.9
E5	DCDC_1v3	O	DCDC_1v3 out	1.3
F3	VDD_DIG	O	VDD_DIG	0.9
G10	VFLASH	O	VFLASH out	1.8
H2	VDD_EXTRA	O	VDD_EXTRA out	1.8
H5	VDD_GPM	O	VDD_GPM out	1.1
K5	VDDIO_GPM	O	VDDIO_GPM out	1.8
L4	VSIM	O	VSIM out	1.8

3.2.2. Power Supply VBAT and VBAT_FEM

The WSCLxADAH2Z needs to connect a DC power supply to VBAT and VBAT_FEM signals.

(1) VBAT

VBAT is a power supply for 1250 (RF (except for FEM)+BB).

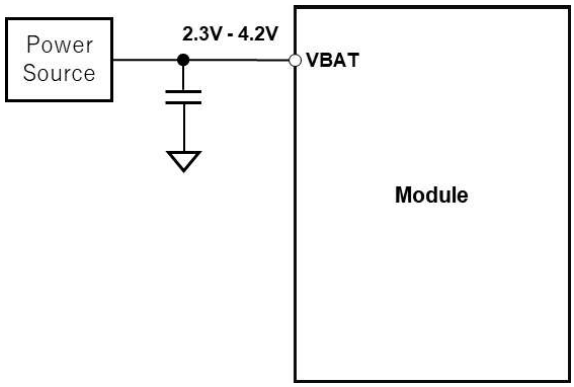


Figure4 VBAT supply block diagram

(2) VBAT_FEM

VBAT_FEM is a power supply for FEM (Front-End Module).

It is to be controlled synchronously with the DRX/ eDRX cycle. See following page for details.

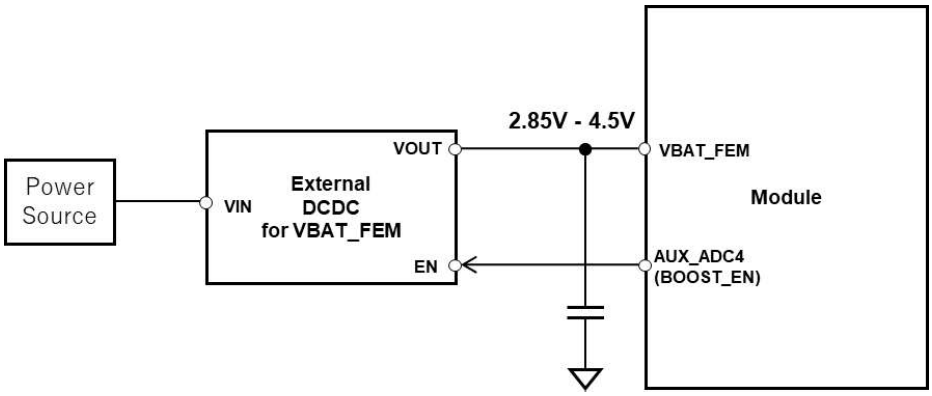


Figure5 VBAT_FEM supply block diagram

When VBAT is 2.3 V (minimum value), must keep 2.3 V or more, during TX.

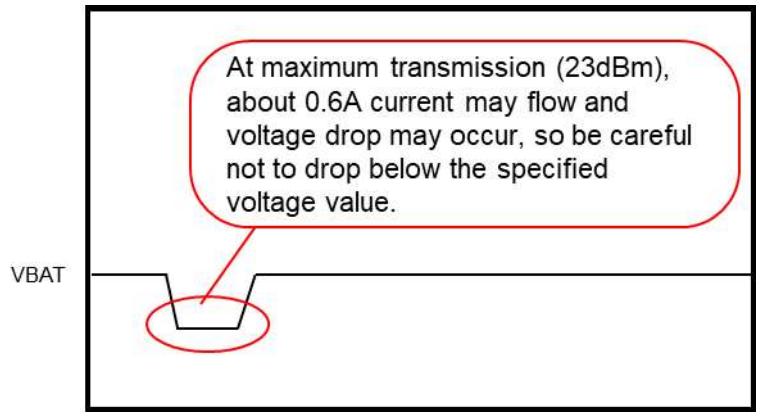


Figure6 drop of power supply voltage (VBAT)

When VBAT_FEM is 2.3 V (minimum value), must keep 2.3 V or more, during TX.

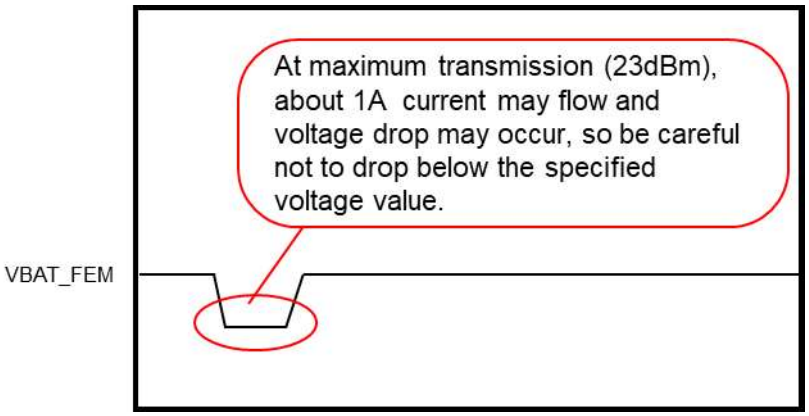


Figure7 drop of power supply voltage (VBAT_FEM)

Figure8 shows reference block diagram of the module.
An external DC-DC converter is required on the VBAT_FEM side of the module.
The reason why the DC-DC converter is necessary is as follows.

- It is synchronizing with eDRX, for power saving.
- The module learns autonomously eDRX cycle.
  AUX_ADC4 (BOOST_EN) synchronizes with eDRX and can control the DC-DC converter.
  (AUX_ADC4 (BOOST_EN) control VBAT_FEM in synchronization with eDRX.)

Figure8 is the recommended circuit. We designed to minimize reduce the current consumption during DH2.

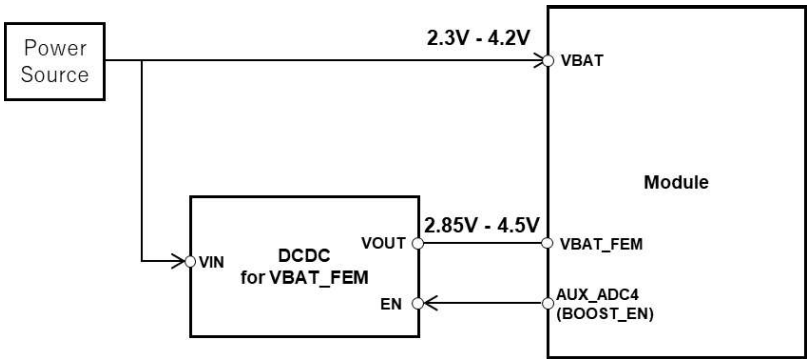


Figure8 reference power block diagram of the module

The external DC-DC converter is TPS61021ADSG.
VBAT_FEM should be supplied by external DC-DC and controlled by ADC_AUX4 (BOOST_EN) pin.

3.2.3. USIM Power Supply VSIM

Through the VSIM power supply interface, 1.8 V power from module can be supplied to USIM card. Special attention should be taken on PCB design at the host side.

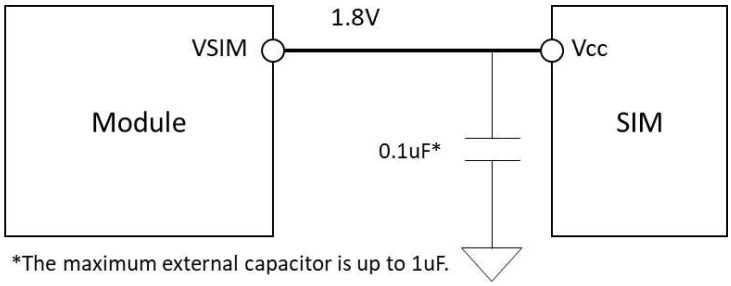


Figure9 VSIM Connection Diagram

3.3. Signal Control Interface

3.3.1. Overview

The external host interface IO in the module includes the following:

- Host Wakeup (SC_SWP pin)
- Module Reset (PMU_SHUTDOOWN pin)
- Module Wakeup (PMU_WAKEUP pin)
- External DCDC Control for FEM (AUX_ADC4 (BOOST_EN) pin)
- Module reset status indicator (SPIM1_CLK pin)

The interface signal voltage is 1.7V to 1.9V.(TYP:1.8V)

Table4 Pins on the signal control interface

Pin No.	PIN Name	I/O	Description
E3	SC_SWP	O	host wakeup 0V=not active (No interrupt) 1.8V=active (Interrupt)
G2	PMU_SHUTDOWN	I	Shutdown, HW reset, active low 0V=active (Module is shutdown) Hi (Pull-up by PMU_VRTC) = not active (Module is active)
G4	PMU_WAKEUP	I	Module wakeup, active high 0V=not active 1.8V=active
F8	AUX_ADC4 (BOOST_EN)	O	1.8V=enable the external DC-DC for VBAT_FEM power
H6	SPIM1_CLK	O	Module reset state indication 1.8V=resetting

3.3.2. SC_SWP Pin

Table5 Two States of SC_SWP Pin

Item	Pin state	Description
1	High	Interrupt to wakeup HOST. 1.8V Module wants to send data to host.
2	Low	No interrupt.

An example of SC_SWP signal connection is shown below.

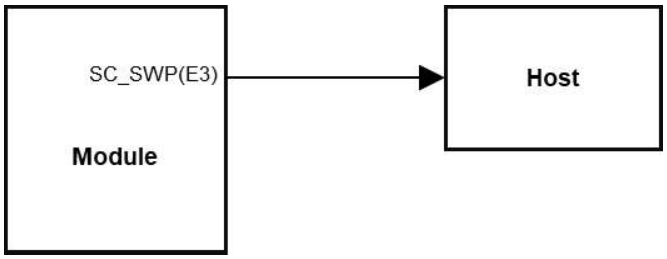


Figure10 SC_SWP signal connection

3.3.3. PMU_SHUTDOWN Pin

This pin requires an external PU resistor (min 600kΩ). Pull source is PMU_VRTC.
This pin has the highest priority compared to other functionalities.
Therefore, it will forcibly hard reset.

Connect this pin to external host with open drain terminal.
To set this pin low level, external host has to output low to this pin.
To set this pin high level, external host does not have to output high. Terminal of host on this pin must be Hi-Z.
Bringing low more than 100us and then bringing high will reset the module.
The PMU_SHUTDOWN pin should not be asserted during the power up and can be used only more than 100msec after VBAT rise above 2.3V.

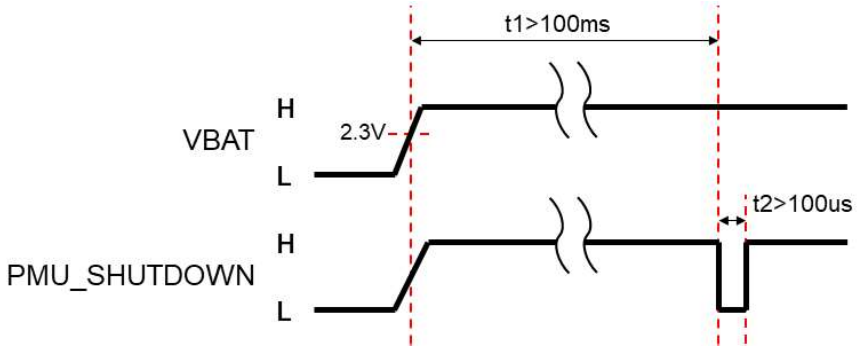


Figure11 PMU_SHUTDOWN pulse width and timing

While VBAT is rising, the HOST does not have to input a signal to the PMU_SHUTDOWN pin, but terminal of HOST on this pin must be Hi-Z. (Please refer to section “6.1.1. Power on”)

Table6 Two States of PMU_SHUTDOWN Pin

Item	Pin state	Description
1	High	Active 1.8V
2	Low	Shutdown

An example of the PMU_SHUTDOWN signal connection is shown below.
(a) is a case where the host interface signal can be Hiz. (b) is an open-drain connection with an external transistor.

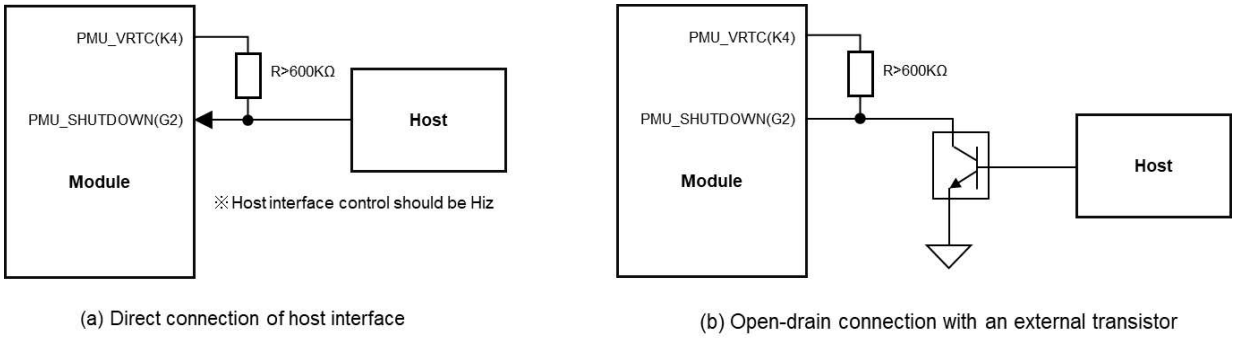


Figure12 PMU_SHUTDOWN signal connection

3.3.4. PMU_WAKEUP Pin

Table7 Two States of PMU_WAKEUP Pin

Item	Pin state	Description
1	High	Wakeup the module or keep active. Module won't enter DH2 if this signal kept high. 1.8V
2	Low	Change the state of module Active to DH2. Note: Never set PMU_WAKEUP to low when the host will send data to the module. (See 6.2. Host-Module Mutual Wakeup Interface)

PMU_WAKEUP signal connection is shown below.

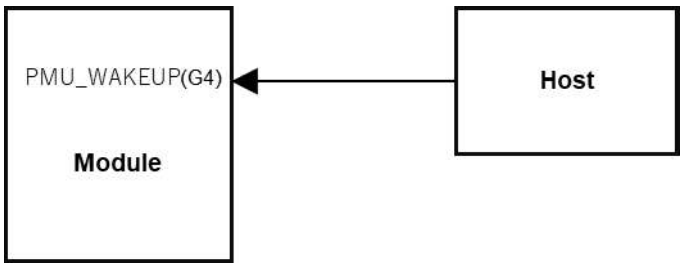


Figure13 PMU_WAKEUP signal connection

3.3.5. AUX_ADC4 (BOOST_EN) Pin

Output signal to enable the external DCDC for VBAT_FEM power.
When AUX_ADC4 (BOOST_EN) pin is to be high, the external DCDC wakes up.
Then VBAT_FEM also wakes up.

Table8 Two States of AUX_ADC4 (BOOST_EN) Pin

Item	Pin state	Description
1	High	Enable 1.8V
2	Low	Disable

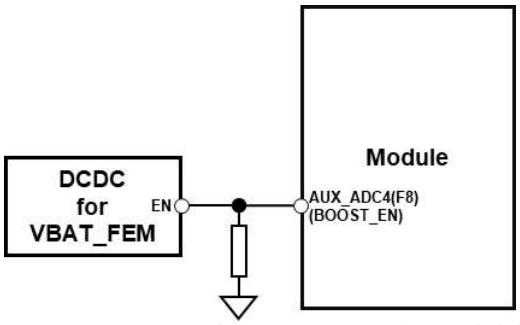


Figure14 connections of the AUX_ADC4 (BOOST_EN) Pin

3.3.6. SPIM1_CLK pin

A signal to indicate that the module is resetting.

Table9 Two States of SPIM1_CLK Pin

Item	Pin state	Description
1	High	Resetting. 1.8V
2	Low	Not in Resetting

SPIM1_CLK signal connection is shown below.

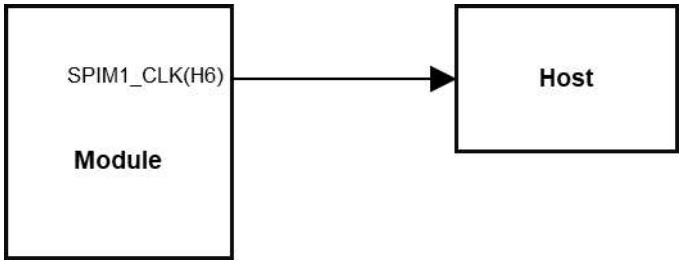


Figure15 SPIM1_CLK signal connection

3.4. UART Interface

The module includes a 4-wire UART interface (UART0 - 2).
The UART is an asynchronous serial interface. The interface is a fully compliant and standard RS-232.
Offers similar functionality to industry-standard 16C550 UART devices.
UART0 is used for AT command or PPP.
* AT command response timeout: max 120s
UART1 is used for debug.
UART2 is used for CLI and firmware version up.

Support baud rates of up to 3Mbps (*). The baud rate can only be changed via AT command. (Refer to Software Application Guide)
The maximum baud rate error is 1.56%.
* Flow control is recommended when the baud rate setting is over 1Mbps.

Default setting is following:
Baud rete: 115200, Data: 8bit, Parity: none, Stop: 1bit, Flow control: none (See Data Format)

[Data Format]

(1) Start bit: start frame transmission (1bit)
(2) Data: length of transmission data in one frame (8bit)
(3) Parity: error detecting code (none)
(4) Stop bit: end frame transmission (1bit)

3.4.1. UART0 Interface

UART0 is used for AT commands and PPP. And connect with the host.

The interface signal voltage is 1.7V to 1.9v.(TYP:1.8V)

Table10 List of UART0 pins

No.	Pin Name	I/O	Description
C8	UART0_RX	I	UART0 receiving data.
D8	UART0_TX	O	UART0 transmitting data.
D9	UART0_CTS(*)	I	UART0 clear to send. 1.8V=active
E8	UART0_RTS(*)	O	UART0 ready to send. 1.8V=active

*If you don't use flow control, you don't need to connect those signals to the host.

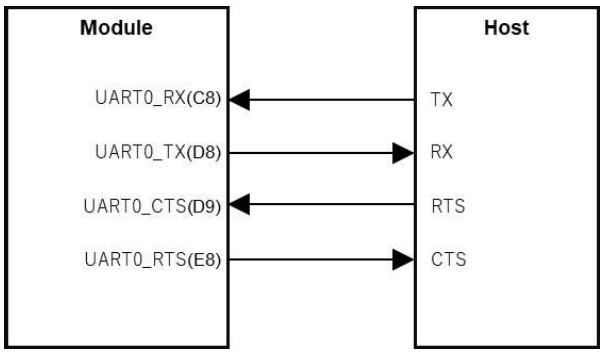


Figure16 UART0 signal connection

3.4.2. UART1,UART2 Interface

UART1, UART2 are manufacturer maintenance ports and are used for debugging and firmware updates.

Special tools are required for data logging and firmware updates.

Please contact your local sales team for tools.

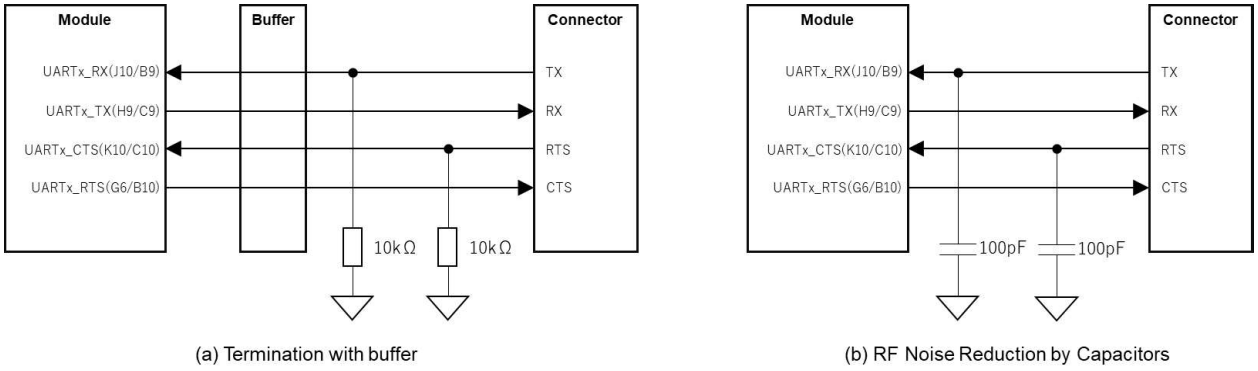
Table11 List of UART1 pins

No.	Pin Name	I/O	Description
J10	UART1_RX	I	UART1 receiving data.
H9	UART1_TX	O	UART1 transmitting data.
K10	UART1_CTS	I	UART1 clear to send. 1.8V=active
G6	UART1_RTS	O	UART1 ready to send. 1.8V=active

Table12 List of UART2 pins

No.	Pin Name	I/O	Description
B9	UART2_RX	I	UART2 receiving data.
C9	UART2_TX	O	UART2 transmitting data.
C10	UART2_CTS	I	UART2 clear to send. 1.8V=active
B10	UART2_RTS	O	UART2 ready to send. 1.8V=active

If the UART1, UART2 signal is open, the module may malfunction due to noise.
Therefore, please take noise countermeasures as follows
It is recommended to connect an external buffer as shown in (a), but if there is no space, etc., please allow for noise reduction with a capacitor as shown in (b).



(a) Termination with buffer

(b) RF Noise Reduction by Capacitors

Figure17 UART1, UART2 signal connection

3.5. USIM Card Interface

The USIM interface can be used either for USIM socket, and for eSIM.
The module supports Class C (1.8V).
For 3.0V USIM cards support, an external voltage translator will be required.
To achieve ultra-low power consumption, SIM power will be off during DH2 mode.
The USIM input/output lines are following USIM specifications.
As the module is not equipped with an USIM card adapter, you need to place an USIM/eSIM card adapter on the user interface board. (Figure 18)
Please design the circuit after evaluating by the customer.
* If you use eSIM, refer to the eSIM datasheet for circuit details.

If you want to use both USIM card adapter and eSIM, please use switch circuit. (Refer to circuit of EVB for detail.)

Table13 List of UART1 pins

No.	Pin Name	I/O	Description
L4	VSIM	O	SIM VCC 1.8V
K3	SIMRST	O	SIM Reset 1.8V
L3	SIMCLK	I	SIM Clock 1.8V
K2	SIMIO	I/O	SIM Data 1.8V It is pulled up with 4.7kΩ by VSIM inside the module.

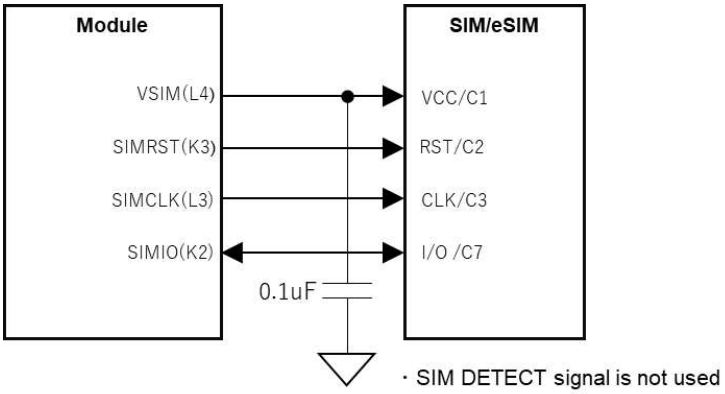


Figure18 USIM Interface signal connection

3.6. RF Antenna Interface

3.6.1. RF Connector location

This module does not include any antennas. External antennas need to be used for the final products using this module.

NOTE

- You should prepare an external antenna which was certified based on the Radio Type Approval of the module.
- Please optimize impedance matching between RF input/output line and antenna by using a matching circuit.
  The RF input/output line of characteristic impedance in the module is 50Ω.
- For recommended antennas, refer to the antenna list (See attachment).

4. RF Specifications

4.1. Operating Frequencies

Table14 shows the RF bands supported by the module

Operating Band	Tx	Rx	Bandwidth	Carrier
Band1	1940MHz - 1960MHz	2130MHz－2150MHz	5MHz /10MHz /15MHz	docomo
Band19	830MHz - 845MHz	875MHz - 890MHz	5MHz /10MHz /15MHz	docomo
Band26	814MHz - 849MHz	859MHz - 894MHz	5MHz /10MHz /15MHz	KDDI

＊For use in Japan only.

4.2. Conducted RF Measurement

4.2.1. RF Test Environment

RF Test instrument	Rohde & Schwarz CMW500
Attenuator	Keysight 8493B

NOTE

- The compensation for different frequency bands relates to the cable and the test environment.
- The instrument compensation needs to be set according to the actual cable conditions.

4.2.2. Test Standards

The module meets 3GPP TS 36.521-1 test standards. The module passes strict tests at the factory and thus the quality of the module is guaranteed.

4.3. RF Specifications

- "Test Value" in the table is the average value of the sample.
- The test values are offset in evaluation board pattern loss.
  Therefore, they are treated as the value of the electrode pad.
- conducted condition
- Temperature: 25 ºC

4.3.1. Rx Sensitivity

Table15 Rx Sensitivity specification

Test Item		Condition	Test Value	3GPP Spec.		Unit
Band	BW		Typ.	Lower	Upper	
1	5MHz	FDD QPSK throughput > 95%	-108.0	-	-103.0	dBm
19	5MHz		-108.0	-	-103.0	dBm
26	5MHz		-108.0	-	-101.0	dBm

4.3.2. Tx Power

Table16 UE Maximum output power

Test Item		Condition		Test Value	3GPP Spec.		Unit
Band	BW			Typ.	Lower	Upper	
1	5MHz	QPSK	1RB	23.0	20.3	25.7	dBm
	10MHz		1RB	23.0	20.3	25.7	dBm
			PRB	23.0	20.3	25.7	dBm
	15MHz		1RB	23.0	20.3	25.7	dBm
			PRB	23.0	20.3	25.7	dBm
19	5MHz	QPSK	1RB	23.0	20.3	25.7	dBm
	10MHz		1RB	23.0	20.3	25.7	dBm
			PRB	23.0	20.3	25.7	dBm
	15MHz		1RB	23.0	20.3	25.7	dBm
			PRB	23.0	20.3	25.7	dBm
26	5MHz	QPSK	1RB	23.0	20.3	25.7	dBm
	10MHz		1RB	23.0	20.3	25.7	dBm
			PRB	23.0	20.3	25.7	dBm

	15MHz		1RB	23.0	20.3	25.7	dBm
			PRB	23.0	20.3	25.7	dBm

Table17 Maximum power reduction (MPR)

Test Item		Condition		Test Value	3GPP Spec.		Unit
Band	BW			Typ.	Lower	Upper	
1	5MHz	QPSK	FRB	22.5	19.3	25.7	dBm
		16QAM	PRB	22.5	19.3	25.7	dBm
			FRB	22.0	18.3	25.7	dBm
	10MHz	QPSK	PRB	23.0	20.3	25.7	dBm
			FRB	22.5	19.3	25.7	dBm
		16QAM	PRB	23.0	20.3	25.7	dBm
			FRB	22.5	19.3	25.7	dBm
	15MHz	QPSK	FRB	23.0	20.3	25.7	dBm
		16QAM	FRB	23.0	20.3	25.7	dBm
19	5MHz	QPSK	FRB	22.5	19.3	25.7	dBm
		16QAM	PRB	22.5	19.3	25.7	dBm
			FRB	22.0	18.3	25.7	dBm
	10MHz	QPSK	PRB	23.0	20.3	25.7	dBm
			FRB	22.5	19.3	25.7	dBm
		16QAM	PRB	23.0	20.3	25.7	dBm
			FRB	22.5	19.3	25.7	dBm
	15MHz	QPSK	FRB	23.0	20.3	25.7	dBm
		16QAM	FRB	23.0	20.3	25.7	dBm
26	5MHz	QPSK	FRB	22.5	19.3	25.7	dBm
		16QAM	PRB	22.5	19.3	25.7	dBm
			FRB	22.0	18.3	25.7	dBm
	10MHz	QPSK	PRB	23.0	20.3	25.7	dBm
			FRB	22.5	19.3	25.7	dBm
		16QAM	PRB	23.0	20.3	25.7	dBm
			FRB	22.5	19.3	25.7	dBm
	15MHz	QPSK	FRB	23.0	20.3	25.7	dBm
		16QAM	FRB	23.0	20.3	25.7	dBm

4.3.3. Frequency Error

Table18 Frequency Error

Test Item		Condition	Test Value	3GPP Spec.		Unit
Band	BW		Typ.	Lower	Upper	
1	5MHz	QPSK-FRB	0.0	-0.1	0.1	ppm
19	5MHz	QPSK-FRB	0.0	-0.2	0.2	ppm
26	5MHz	QPSK-FRB	0.0	-0.2	0.2	ppm

4.3.4. EVM

Table19 EVM

Test Item		Condition	Test Value	3GPP Spec.		Unit
Band	BW		Typ.	Lower	Upper	
1	5MHz	Max Pwr; QPSK-PRB	10.0	-	17.5	%rms
		Max Pwr; QPSK-FRB	10.0	-	17.5	%rms
		Max Pwr; 16QAM-PRB	8.0	-	12.5	%rms
		Max Pwr; 16QAM-FRB	8.0	-	12.5	%rms
19	5MHz	Max Pwr; QPSK-PRB	10.0	-	17.5	%rms
		Max Pwr; QPSK-FRB	10.0	-	17.5	%rms
		Max Pwr; 16QAM-PRB	8.0	-	12.5	%rms
		Max Pwr; 16QAM-FRB	8.0	-	12.5	%rms
26	5MHz	Max Pwr; QPSK-PRB	10.0	-	17.5	%rms
		Max Pwr; QPSK-FRB	10.0	-	17.5	%rms
		Max Pwr; 16QAM-PRB	8.0	-	12.5	%rms
		Max Pwr; 16QAM-FRB	8.0	-	12.5	%rms

4.3.5. Carrier Leakage

Table20 Carrier Leakage

Test Item		Condition	Test Value	3GPP Spec.		Unit
Band	BW		Typ.	Lower	Upper	
1	5MHz	3.2dBm, QPSK-PRB	-36.0	-	-24.2	dBc
19	5MHz	3.2dBm, QPSK-PRB	-36.0	-	-24.2	dBc
26	5MHz	3.2dBm, QPSK-PRB	-36.0	-	-24.2	dBc

4.3.6. Occupied Bandwidth

Table21 Occupied Bandwidth

Test Item		Condition	Test Value	3GPP Spec.		Unit
Band	BW		Typ.	Lower	Upper	
1	5MHz	QPSK-FRB	1.05	-	1.40	MHz
19	5MHz	QPSK-FRB	1.05	-	1.40	MHz
26	5MHz	QPSK-FRB	1.05	-	1.40	MHz

4.3.7. Adjacent Channel power

Table22 Adjacent Channel Power (Band1)

Modulation	BW	Condition	Test Value (Typ.)	3GPP Spec.		Unit
				Lower	Upper	
QPSK	5MHz	EUTRA @-5MHz	36.0	29.2	-	dB
		EUTRA @5MHz	36.0	29.2	-	
		UTRA @-10MHz	50.0	35.2	-	
		UTRA @-5MHz	40.0	35.2	-	
		UTRA @5MHz	40.0	32.2	-	
		UTRA @10MHz	50.0	35.2	-	
	10MHz	EUTRA @-10MHz	36.0	29.2	-	dB
		EUTRA @10MHz	36.0	29.2	-	
		UTRA @-12.5MHz	50.0	35.2	-	
		UTRA @-7.5MHz	40.0	32.2	-	
		UTRA @7.5MHz	40.0	32.2	-	
		UTRA @12.5MHz	50.0	35.2	-	
	15MHz	EUTRA @-15MHz	36.0	29.2	-	dB
		EUTRA @15MHz	36.0	29.2	-	
		UTRA @-15MHz	50.0	35.2	-	
		UTRA @-10MHz	40.0	32.2	-	
		UTRA @10MHz	40.0	32.2	-	
		UTRA @15MHz	50.0	35.2	-	
16QAM	5MHz	EUTRA @-5MHz	36.0	29.2	-	dB
		EUTRA @5MHz	36.0	29.2	-	
		UTRA @-10MHz	50.0	35.2	-	
		UTRA @-5MHz	40.0	32.2	-	
		UTRA @5MHz	40.0	32.2	-	

		UTRA @10MHz	50.0	35.2	-	
	10MHz	EUTRA @-10MHz	36.0	29.2	-	dB
		EUTRA @10MHz	36.0	29.2	-	
		UTRA @-12.5MHz	50.0	35.2	-	
		UTRA @-7.5MHz	40.0	32.2	-	
		UTRA @7.5MHz	40.0	32.2	-	
		UTRA @12.5MHz	50.0	35.2	-	
	15MHz	EUTRA @-15MHz	36.0	29.2	-	dB
		EUTRA @15MHz	36.0	29.2	-	
		UTRA @-15MHz	50.0	35.2	-	
		UTRA @-10MHz	40.0	32.2	-	
		UTRA @10MHz	40.0	32.2	-	
		UTRA @15MHz	50.0	35.2	-	

Table24 Adjacent Channel Power (Band19)

Modulation	BW	Condition	Test Value (Typ.)	3GPP Spec.		Unit
				Lower	Upper	
QPSK	5MHz	EUTRA @-5MHz	36.0	29.2	-	dB
		EUTRA @5MHz	36.0	29.2	-	
		UTRA @-10MHz	50.0	35.2	-	
		UTRA @-5MHz	40.0	32.2	-	
		UTRA @5MHz	40.0	32.2	-	
		UTRA @10MHz	50.0	35.2	-	
	10MHz	EUTRA @-10MHz	36.0	29.2	-	dB
		EUTRA @10MHz	36.0	29.2	-	
		UTRA @-12.5MHz	50.0	35.2	-	
		UTRA @-7.5MHz	40.0	32.2	-	
		UTRA @7.5MHz	40.0	32.2	-	
		UTRA @12.5MHz	50.0	35.2	-	
	15MHz	EUTRA @-15MHz	36.0	29.2	-	dB
		EUTRA @15MHz	36.0	29.2	-	
		UTRA @-15MHz	50.0	35.2	-	
		UTRA @-10MHz	40.0	32.2	-	
		UTRA @10MHz	40.0	32.2	-	
		UTRA @15MHz	50.0	35.2	-	
16QAM	5MHz	EUTRA @-5MHz	36.0	29.2	-	dB
		EUTRA @5MHz	36.0	29.2	-	

		UTRA @-10MHz	50.0	35.2	-	
		UTRA @-5MHz	40.0	32.2	-	
		UTRA @5MHz	40.0	32.2	-	
		UTRA @10MHz	50.0	35.2	-	
	10MHz	EUTRA @-10MHz	36.0	29.2	-	
		EUTRA @10MHz	36.0	29.2	-	
		UTRA @-12.5MHz	50.0	35.2	-	
		UTRA @-7.5MHz	40.0	32.2	-	dB
		UTRA @7.5MHz	40.0	32.2	-	
		UTRA @12.5MHz	50.0	35.2	-	
	15MHz	EUTRA @-15MHz	36.0	29.2	-	
		EUTRA @15MHz	36.0	29.2	-	
		UTRA @-15MHz	50.0	35.2	-	
		UTRA @-10MHz	40.0	32.2	-	dB
		UTRA @10MHz	40.0	32.2	-	
		UTRA @15MHz	50.0	35.2	-	

Table25 Adjacent Channel Power (Band26)

Modulation	BW	Condition	Test Value (Typ.)	3GPP Spec.		Unit
				Lower	Upper	
QPSK	5MHz	EUTRA @-5MHz	36.0	29.2	-	
		EUTRA @5MHz	36.0	29.2	-	
		UTRA @-10MHz	50.0	35.2	-	
		UTRA @-5MHz	40.0	32.2	-	dB
		UTRA @5MHz	40.0	32.2	-	
		UTRA @10MHz	50.0	35.2	-	
	10MHz	EUTRA @-10MHz	36.0	29.2	-	
		EUTRA @10MHz	36.0	29.2	-	
		UTRA @-12.5MHz	50.0	35.2	-	
		UTRA @-7.5MHz	40.0	32.2	-	dB
		UTRA @7.5MHz	40.0	32.2	-	
		UTRA @12.5MHz	50.0	35.2	-	
	15MHz	EUTRA @-15MHz	36.0	29.2	-	
		EUTRA @15MHz	36.0	29.2	-	
		UTRA @-15MHz	50.0	35.2	-	
		UTRA @-10MHz	40.0	32.2	-	dB
		UTRA @10MHz	40.0	32.2	-	

		UTRA @15MHz	50.0	35.2	-	
16QAM	5MHz	EUTRA @-5MHz	36.0	29.2	-	dB
		EUTRA @5MHz	36.0	29.2	-	
		UTRA @-10MHz	50.0	35.2	-	
		UTRA @-5MHz	40.0	32.2	-	
		UTRA @5MHz	40.0	32.2	-	
		UTRA @10MHz	50.0	35.2	-	
	10MHz	EUTRA @-10MHz	36.0	29.2	-	dB
		EUTRA @10MHz	36.0	29.2	-	
		UTRA @-12.5MHz	50.0	35.2	-	
		UTRA @-7.5MHz	40.0	32.2	-	
		UTRA @7.5MHz	40.0	32.2	-	
		UTRA @12.5MHz	50.0	35.2	-	
	15MHz	EUTRA @-15MHz	36.0	29.2	-	dB
		EUTRA @15MHz	36.0	29.2	-	
		UTRA @-15MHz	50.0	35.2	-	
		UTRA @-10MHz	40.0	32.2	-	
		UTRA @10MHz	40.0	32.2	-	
		UTRA @15MHz	50.0	35.2	-	

5. Electrical Specifications

5.1. Absolute Maximum Ratings

WARNING

Table26 lists the absolute ratings for the module. Using the module beyond these conditions may result in permanent damage to the module.

Table26 Absolute maximum ratings for the module

Symbol	Parameter	Min.	Max.	Unit
VBAT	VBAT supply pin	-0.3	4.5	V
VBAT_FEM	RF supply pin	-0.3	4.5	V

5.2. Operating Conditions

Table27 Operating conditions

Parameter	Min.	Typ.	Max.	Unit	Condition
Operating temperatures	-30		+70	ºC	*1-
Storage temperatures	-40	-	+80	ºC	-
Module Vin (VBAT)	2.3	-	4.35	V	*2
Module Vin (VBAT_FEM)	2.3	-	4.35	V	-
VBAT_FEM Rise Time	-	-	1	ms	from power on to 2.2V

*1: 3GPP release 13 compliant

*2: VBAT slew rate should be less than 25mV/us

Table28 DC Characteristics of pins

Parameter	Min.	Max.	Unit
V_{IH}	0.7 * V_{IO}	-	V
V_{IL}	-	0.3 * V_{IO}	V
V_{OH}	0.8 * V_{IO}	-	V
V_{OL}	-	0.2 * V_{IO}	V
V_{IO}	1.7	1.9	V

VIO is generated by the module's internal LDO

5.3. Conducted Electrical Measurement

5.3.1. Electrical Test Environment

Test instrument	Keysight N6705B、Keysight N6781A

5.4. Power Supply

5.4.1. Input Power Supply

Table29 Requirements for input power of the module

Parameter	Min.	Max.	Ripple Max.	Unit
VBAT	2.3	4.35	50mVpp	V
VBAT_FEM	2.3	4.35	50mVpp	V

Table30 Maximum Current Ratings

Supply Name	Description	Max	Unit
VBAT	Maximum current rating for the VBAT domain	0.6	A
VBAT_FEM	Maximum current rating for the FEM domain	1	A

5.4.2. Power State

Module is optimized to achieve ultra-low power consumption addressing IoT market needs. Power state is supported. (See the following Table31)

Table31 Power state

Power state	Description	Required supplies	Wake-up options
Shutdown	Module powered off.	-	-
DH2 *	All digital logic is powered down, a configurable amount of retention memory is retained (64KB granularity), all output IOs are latched while input IOs can be configured to wake up the system, and the RTC is 'On' in this mode. IO Retention, SW state Full Retention, Memory Partially Retention, Timer IO's Note: In this mode VDDIO_GPM keeps turned on.	-	RTC Expiration PMU_WAKEUP PMU_SHUTDOWN Any other digital interface configured to wakeup the system A wakeup event initiates a boot flow. This mode enables output IOs to latch and wakeup from digital input.
Active	All system is wake up.	All required power supplies are available.	-

*DH2 = Deep Hibernation mode 2. Generally, it means Sleep (eDRX/DRX) state.

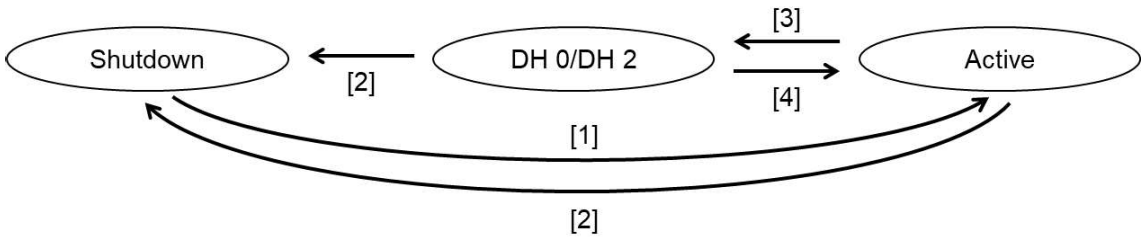


Figure19 power state transition diagram

NOTE

Related procedures are described in order sections;

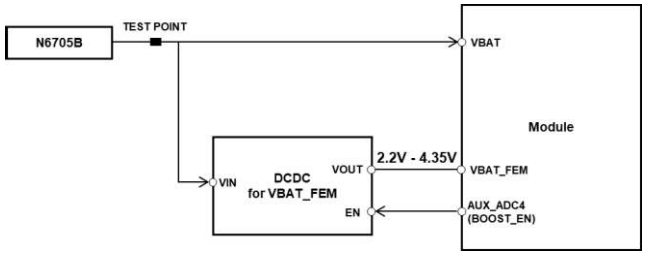
[1] Shutdown --> Active: See 6.1. Power on/off sequence
See 6.2.1. Open data interface -host to module

[2] Active or DH 2 --> Shutdown: See 6.1. Power on/off sequence

[3] Active --> DH 2: See 6.2.3. Close data interface

[4] DH 2 --> Active: See 6.2.1. Open data interface -host to module
See 6.2.2. Open data interface -module to host

5.4.3. Power Consumption



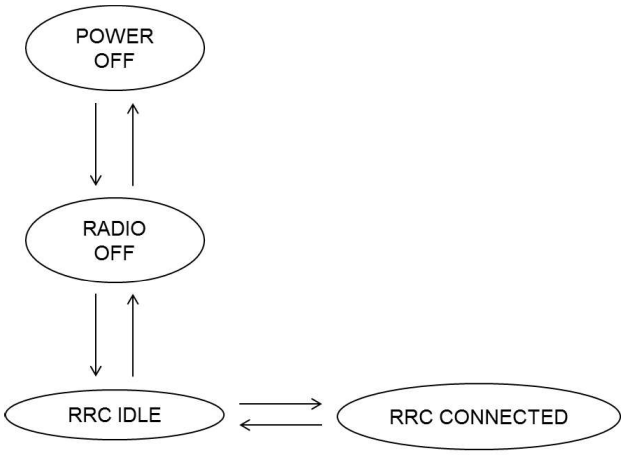
[conditions]

- measured on our evaluation board at 25ºC indoor
- Band: 1, Band Width: 5MHz
- DRX cycle = 1.28 s
- eDRX cycle = 81.92s, PTW = 1.28 s
- power supply of the module is 3.0V

Table32 Averaged power consumption of the evaluation board

wireless state	power state	Typical values (Avg)	Notes/Condition
RRC CONNECTED	Active	195mA	Tx Power: 0dBm
		233mA	Tx Power: 10dBm
		543mA	Tx Power: 23dBm
	DH2	1.4mA	DRX [1] (SIM power on)
		50uA	eDRX [2] Average power consumption for 1 hour after shift to eDRX.

* It may be changed because of under development.



POWER OFF : Module switched off
RADIO OFF : RF is disabled
RRC IDLE : RF is enabled
RRC CONNECTED : During transmitting and receiving data

Figure20 wireless state transition diagram

[1] image of current waveform during DRX

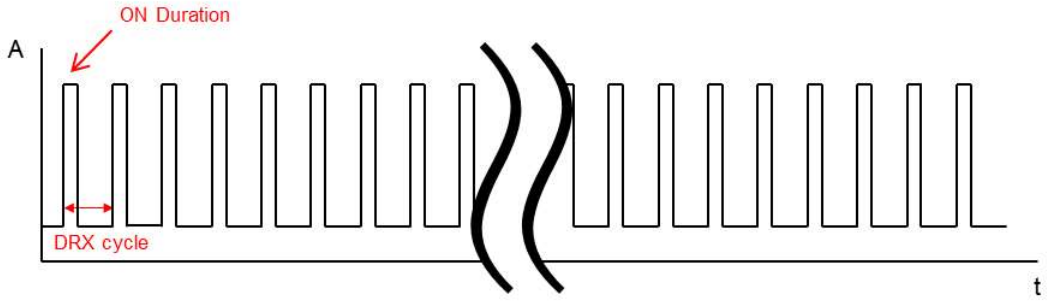


Figure21 image of current waveform during DRX

[2] image of current waveform during eDRX

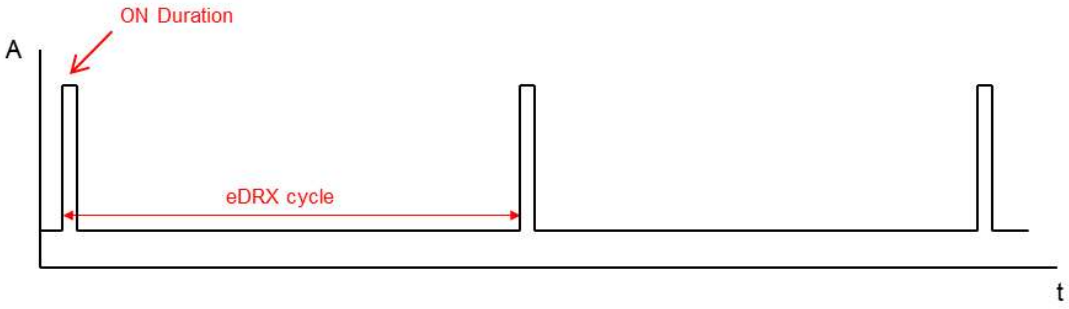


Figure22 image of current waveform during eDRX

5.4.4. AC Electrical Specifications

See Table 33 for the rise and fall of digital signals.

Table33 Digital signals rising & falling time

Min. – 1.7V , -40C , Typ. – 1.8V , 25C , Max. – 1.9V , 85C

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
Tr	Pin Rise Time	DS (Drive Strength) = 4mA, CL=10pF SR(Slew Rate) = Slow	0.4	0.8	1.3	ns
Tf	Pin Fall Time	DS (Drive Strength) = 4mA, CL=10pF SR(Slew Rate) = Slow	0.4	0.7	1.2	ns

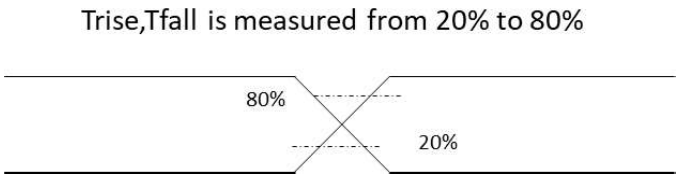


Table34 PMU Analog Pins' specifications

Symbol	Parameter	Min.	Max.	Unit
WK_VIL	Input LOW level, PMU_WAKEUP	-	0.3	V
WK_VIH	Input HIGH level, PMU_WAKEUP	1.2	-	V
SD_VIL	Input LOW level, PMU_SHUTDOWN	-	0.3	V
SD_VIH	Input HIGH level, PMU_SHUTDOWN	1.3	-	V
WK_T	The minimum assertion time to wake up the device, PMU_WAKEUP	100	-	us
SD_T	The minimum assertion time to perform a hard reset of the PMU, PMU_SHUTDOWN	100	-	us

6. Function and Features

6.1. Power on/off

6.1.1. Power on

The module is powered-on triggered by inputting VBAT. VBAT should rise from less than 0.15V. When the module is powered, PMU_VRTC rises. At the same time, PMU_SHUTDOWN signal rises as it is pulled up to PMU_VRTC outside the module. While VBAT is rising, HOST does not need to input a signal to the PMU_SHUTDOWN pin, terminal of HOST must be Hi-Z on this pin.

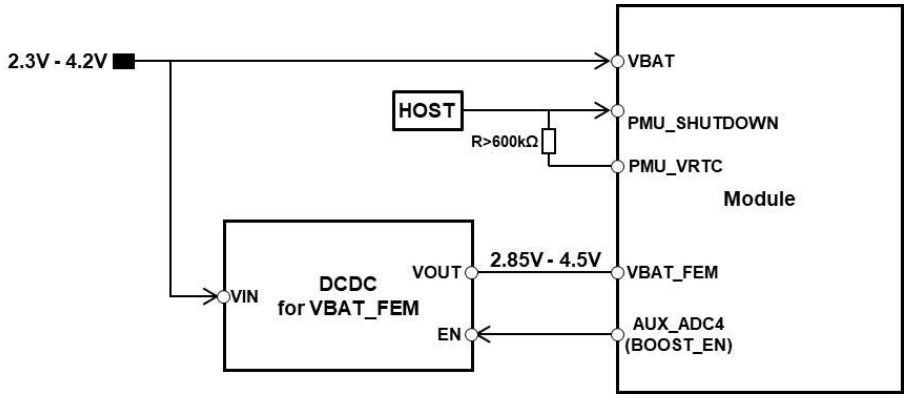


Figure23 reference block diagram of power on

NOTE

● Since the VBAT slew rate should be less than 25mV/us, it is recommended to use a load switch or power supply for the rise time of VBAT to be adjustable.

● The operating voltage of VBAT is minimum 2.3V, so the rise time of VBAT should be 92uS or more between 0 and 2.3V.

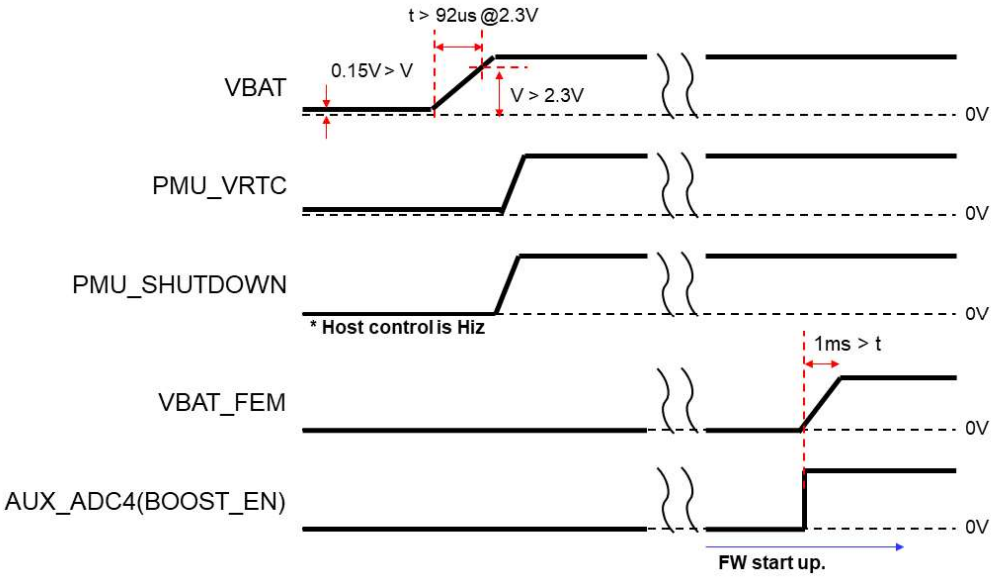
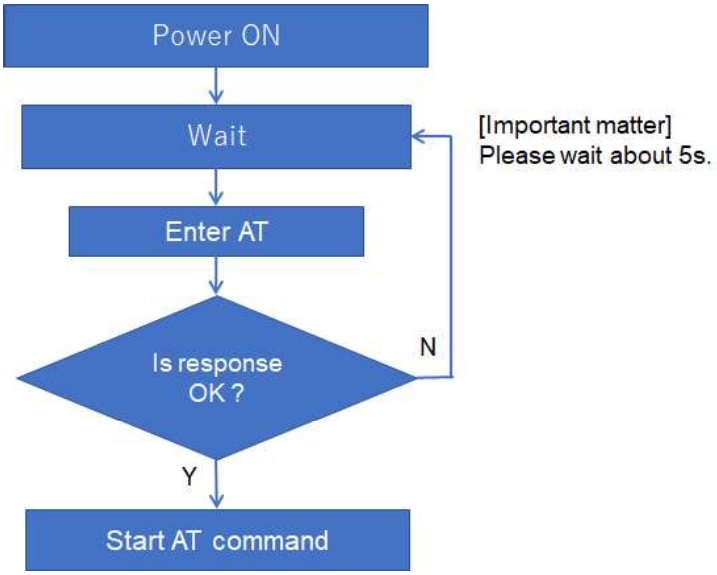


Figure24 power on sequence

- A flowchart showing start AT command.



6.1.2. Power off

The module is powered off when VBAT falls.
Terminal of HOST on PMU_SHUTDOWN pin should be Hi-Z while VBAT is falling.
PMU_SHUTDOWN and PMU_VRTC fall simultaneously.

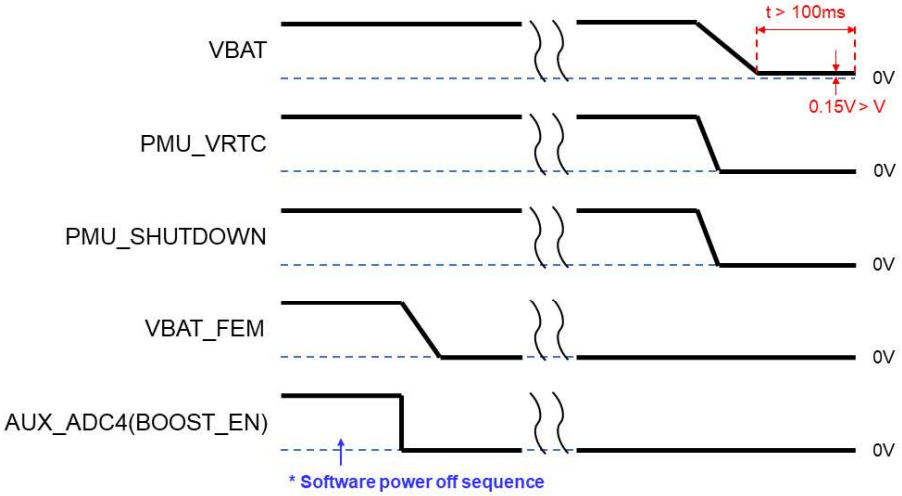


Figure25 power off sequence

NOTE

- Do not power off during module boot.
  If power off during access to flash, module may break.
- After execute software power off sequence (AT Command), VBAT turn off.
  Refer to the following document for the software power off sequence.
  - Cat-M1_Software_Application_Guide ("3.4. Modem Function OFF")

6.2. Host-Module Mutual Wakeup Interface

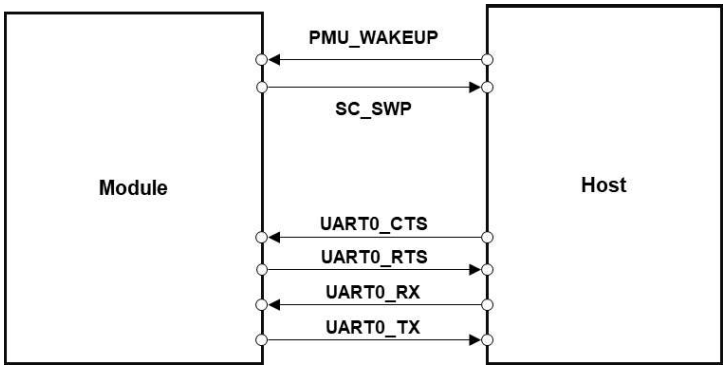


Figure26 Host-Module mutual wakeup

The state of PMU_WAKEUP and SC_SWP

(1) PMU_WAKEUP (Host: Output, Module: Input)

High：When host need to open the data interface and to wake up to module.

Low：When host need to close the data interface.

(2) SC_SWP (Host: Input, Module: Output)

High：Module need to open the data interface.

Therefore, interrupt to wakeup host.

Low：Module do not need to open the data interface.

Table35 the requirements for the external host interface IO

No.	Pin Name	Description
G4	PMU_WAKEUP	host wakes up module
E3	SC_SWP	module wakes up host
D8	UART0_TX	UART0 transmitting data
C8	UART0_RX	UART0 receiving data
E8	UART0_RTS	UART0 ready to send
D9	UART0_CTS	UART0 clear to send
G2	PMU_SHUTDOWN	hardware reset

*: Connect these pins to pins header etc.

6.2.1. Open data interface -host to module

When host wants to send data to module, host should open data interface.
The timing chart is as follows. (See Figure30)

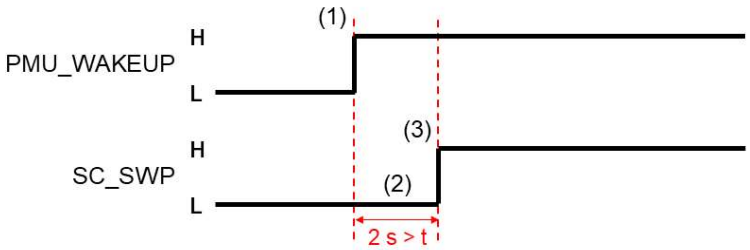


Figure27 open data interface - host to module

First, data interface state is not open.
UART0_RX and UART0_TX are always high.
(1) Host wants to send data to module. Host sets PMU_WAKEUP to high (PMU_WAKEUP = high)
(2) Module is awaking (might also be waking) and module is preparing
(3) Module sets SC_SWP to high (SC_SWP = high)
The data interface is opened and communication can start

6.2.2. Open data interface –module to host

When module wants to send data to host, module opens data interface.

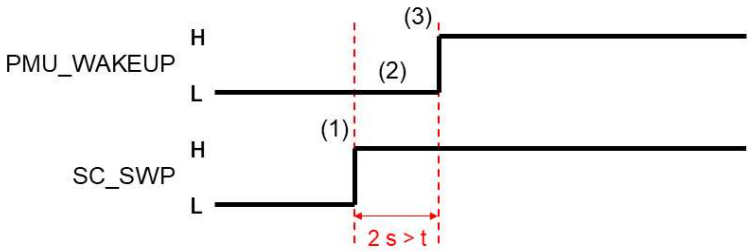


Figure28 open data interface - module to host

First, data interface state is not open.
UART0_RX and UART0_TX are always high.

(1) Module wants to send data to host. Module sets SC_SWP to high (SC_SWP = high)
(2) When host detects module sets SC_SWP to high, host needs to do the processing necessary to receive data
(3) When host is completed the processing on UART, host sets PMU_WAKEUP to high (PMU_WAKEUP = high)

The data interface is opened and communication can start

6.2.3 Close data interface

Host has no send data and wants to close data interface.
Then shift the state of module Active to DH2.

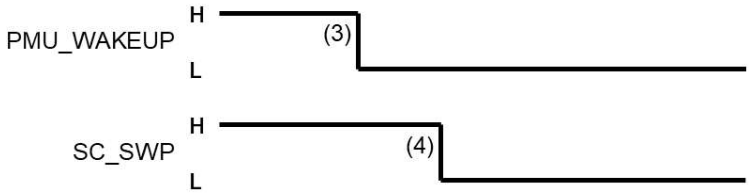


Figure29 close data interface

UART0_RX and UART0_TX are always high.
(1) Host detects that it is sending the last data bit in a session and module is not transmitting any data (UART0_TX = high)
(2) Host will not send any data (UART0_RX = fix = high)
(3) Host sets PMU_WAKEUP to low (PMU_WAKEUP = low)
(4) Module detects PMU_WAKEUP is low, and sets SC_SWP to low (SC_SWP = low)
The point is, the data interface closes and the module will sleep

NOTE

When there are events on the LTE network, Module does not sleep.
(e.g. RRC status is RRC-connected)

In that case, wait for the end of the communication event.
Since it is necessary to receive the output data of the module.
Please resume data connection.

The following figure shows the flowchart of close data interface.

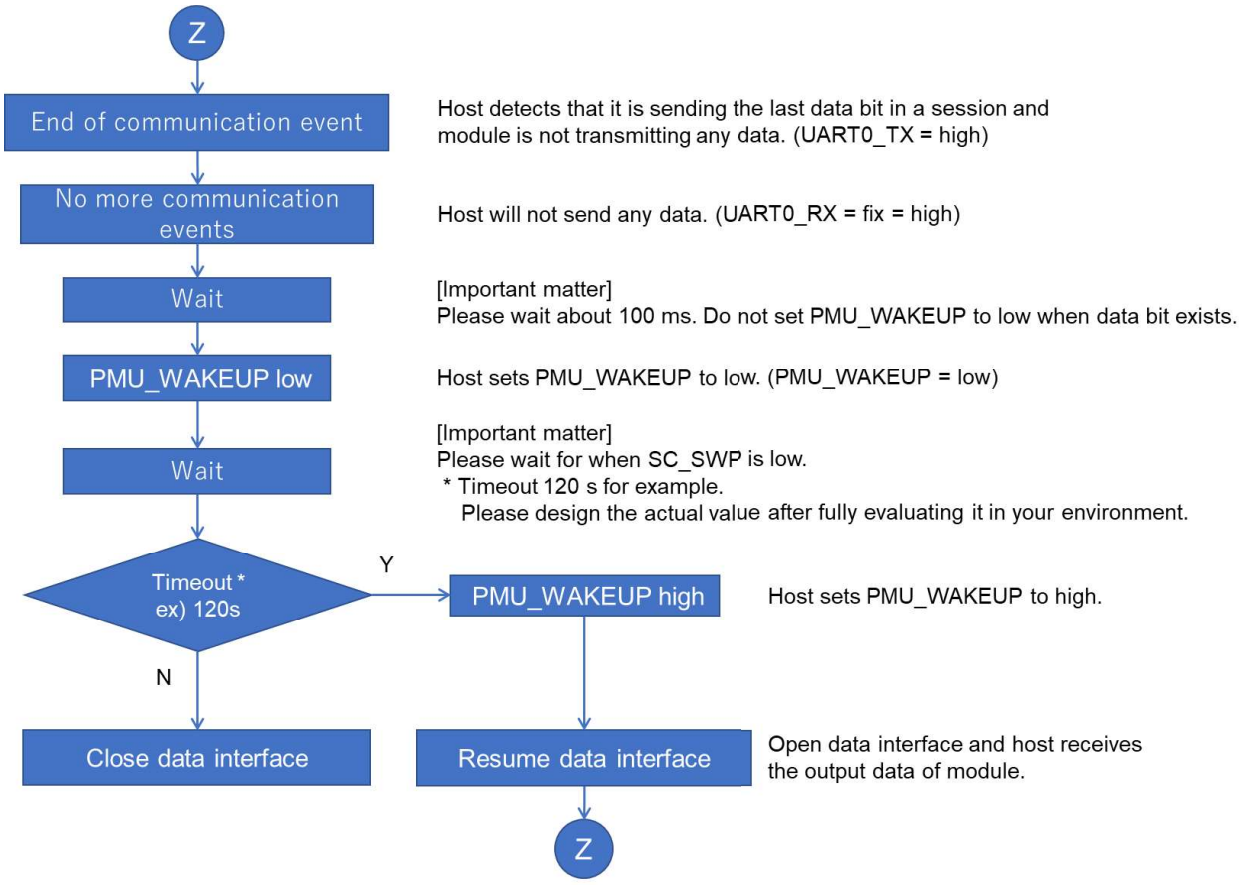


Figure30 flowchart of close data interface

6.3. Detect reset of module

When module boot/reboot, high pulse on SPIM_CLK (H6) output for 2s (*).

* 2s = default value.

NOTE

- Output time of reset pulse is equal to setting value of AT%SETBDELAY.
  You change the output time, boot time is changed too.
- The reset notification function cannot be disabled.
- The reset signal is output even when the module is in the sleep state (=PMU_WAKEUP is Low)

6.4. Basic Reliability Features

Table36 Test conditions and results of the reliability of the module

Item	Test Condition	Results
High-Temperature Storage Test	Devices are left for 2 hours in the normal temperature and humidity after being placed in a high temperature (80℃) environment for 100 hours, while no voltage is applied.	Devices should show no abnormal electrical performance.
Low-Temperature Storage Test	Devices are left for 2 hours in the normal temperature and humidity after being placed in a low temperature (-40℃) environment for 100 hours, while no voltage is applied.	Devices should show no abnormal electrical performance.
High-Temperature and Humidity Storage Test	Devices are left for 2 hours in the normal temperature and humidity after being exposed to 95% humidity at 85℃ for 100 hours, while no voltage is applied.	Devices should show no abnormal electrical performance.
Thermal Shock Test (Air)	Devices are left for 2 hours in the normal temperature and humidity after being placed at two different temperature [-40~(transition time max.10Sec.) 85℃] in the atmosphere for 30 minutes respectively and this cycle is repeated 300 times.	Devices should show no abnormal electrical performance.
High Temperature Test (Biased)	After being placed in a high temperature (75℃) environment for 100 hours, while receiving and transmitting, the device is measured in the same environment.	Devices should show no abnormal electrical performance.
Humidity Test (Biased)	Devices are left for 2~24 hours in the normal temperature and humidity after being exposed to 95% humidity at 60℃ for 100 hours, operating the receiver and transmitter electric circuit of devices.	Devices should show no abnormal electrical performance.
ESD (Machine Model)	C = 200pF, R = 0 ohm, +/-100V, 5 times for each terminal ESD was applied to all module terminals except GND.	Devices should show no abnormal electrical performance.
Solder Heat Resistance Test	Peak temperature 250℃ (+5/-0℃), 2 times	Devices should show no abnormal electrical performance.
Vibration Test (Device)	Devices are fixed to a vibration table. overall amplitude of vibration:1.5mm at f=10~82Hz acceleration of vibration:196m/s^2 20G at f=82~2000Hz, sweep time:4 minutes (f=10~2000~10Hz) X, Y and Z-axis for 2 hours each for a total of 6 hours.	Devices should show no abnormal electrical performance.
Free Fall Test	Devices will be dropped naturally on the concrete board 6 faces*3 times at a height of 75 centimeter.	Devices should show no abnormal electrical performance.

7. Mechanical Specifications

7.1. Dimensions of the module

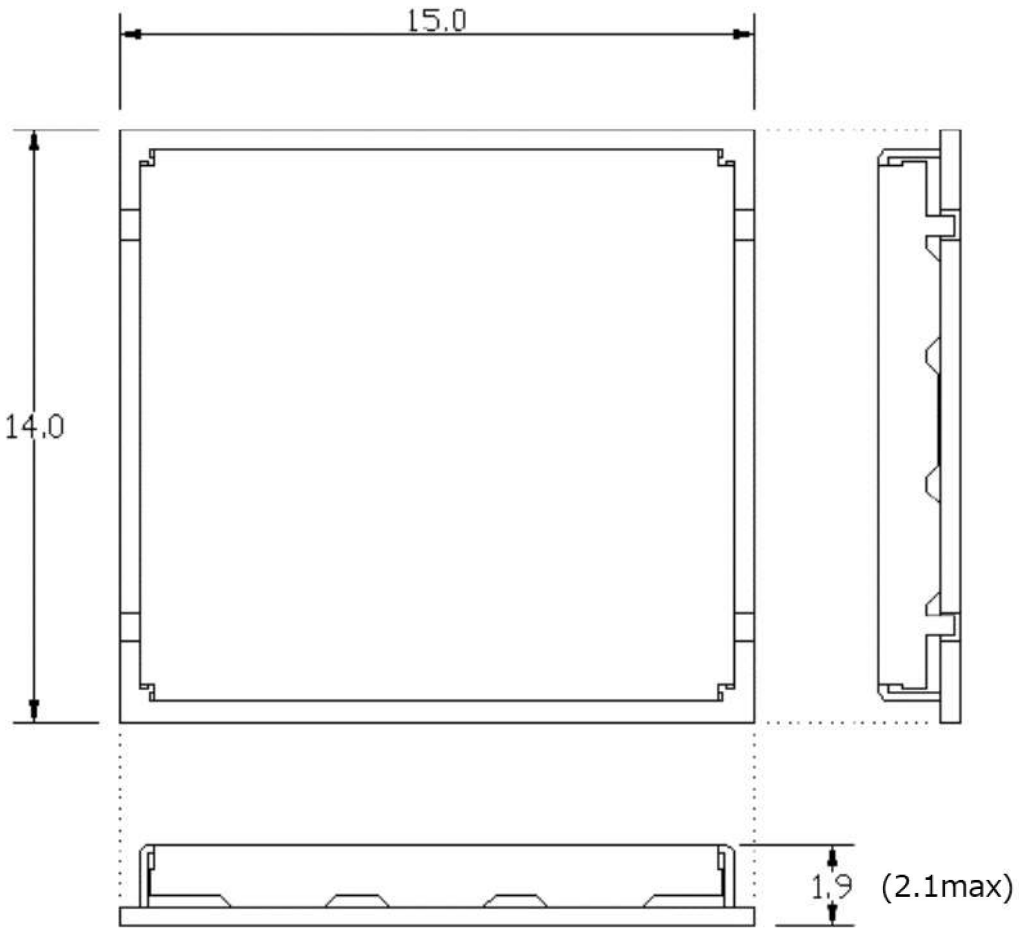


Figure31 dimensions of the module (TOP VIEW) (unit: mm)

*Tolerances unless otherwise specified: ±0.2mm

Unit: mm, Tolerances unless otherwise specified: ±0.2mm
単位: mm, 指示無公差: ±0.2mm

Coplanarity : ±0.1mm
端子平坦度 : ±0.1mm

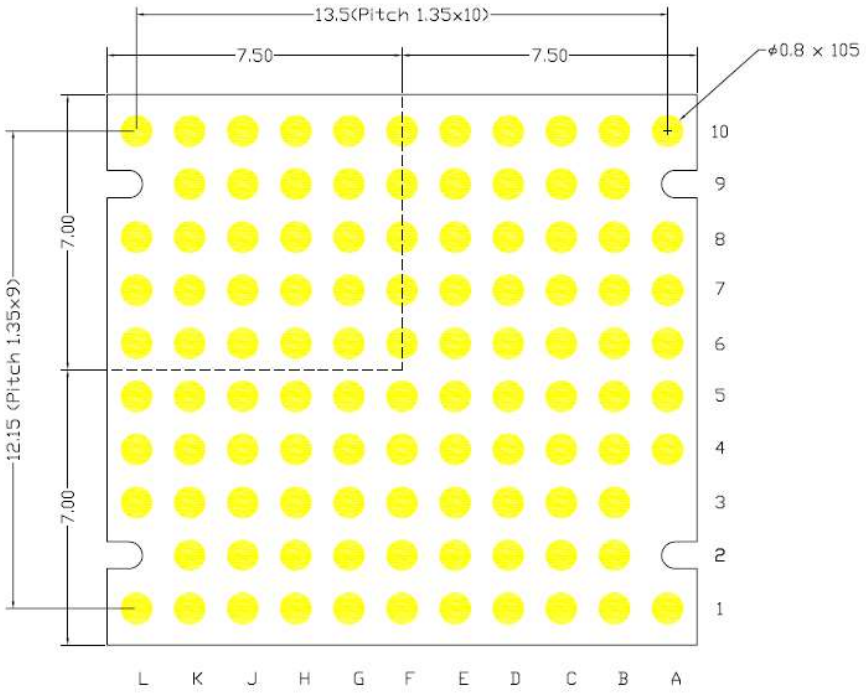
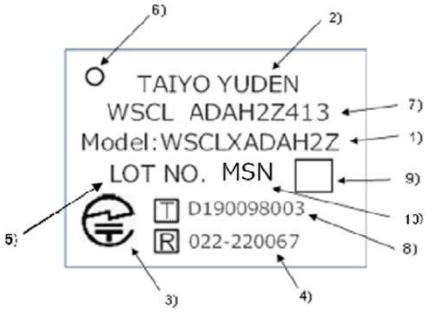


Figure32 Dimensions of the module (TOP THRU VIEW) (unit: mm)

7.2. Label



1) Model	: WSCLxADAH2Z
2) Manufacture	: TAIYO YUDEN
3) Japan logo mark	: Specified logo mark
4) Japan ID	: Specified ID Number
5) Lot number	: Four digits
6) 1Pin mark	: ϕ1.0mm circle mark on the shield case
7) Type	: WSCL2ADAH2Z413 / WSCL3ADAH2Z413
8) JATE ID	: Specified ID Number
9) QR Code	: Process control code
10) MSN	: Manufacturing Serial Number

EX) 2N410 12345
Lot MSN

MSN (1-digit JEMS control number, space, 5-digit JEMS serial number) is displayed following the 4-digit lot number

Figure33 description of label

7.3. Packing System

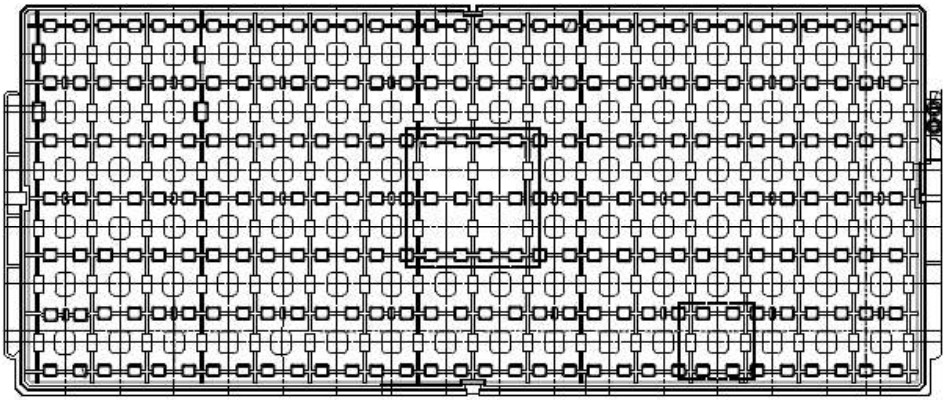
Table 37 Packaging Material

Name	Outline	Materials	Note
Tray	315 × 135.9 × 7.62 (mm)	Conductive PPE	96 pieces/tray
Antistatic band	8mm wide	Antistatic PP	-
Desiccant	-	Desi-Pak	-
Humidity indicator card	-	-	-
Aluminum moisture barrier bag	260 × 460 (mm)	(AS)PET/AL/NY/PE(AS)	-
Buffer corrugated paper	-	Corrugated fiberboard	-
Label	-	-	-
Caution Label	-	-	-
Inner box	345 × 205 × 95 (mm)	Corrugated fiberboard	-

The module package includes the tray, tray(cover), antistatic band, desiccant, and humidity indicator card.
This module is stored in the tray in units of 96 pieces.

- Packaging method: Tray
- Packaging unit: 960

  * It might be providing as tray at sample stage.



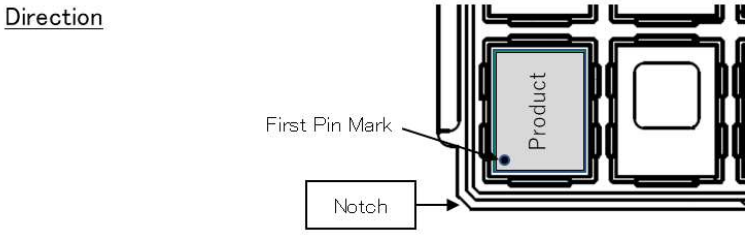


Figure34 packaging Figure

Place 10 trays, place the tray (cover) on it, and place it in an aluminum moisture barrier bag together with desiccant and humidity indicator card.
Both ends of the aluminum moisture barrier bags are sandwiched by buffer corrugated paper and placed in the inner box.
The interior box is packed in an exterior box and shipped.

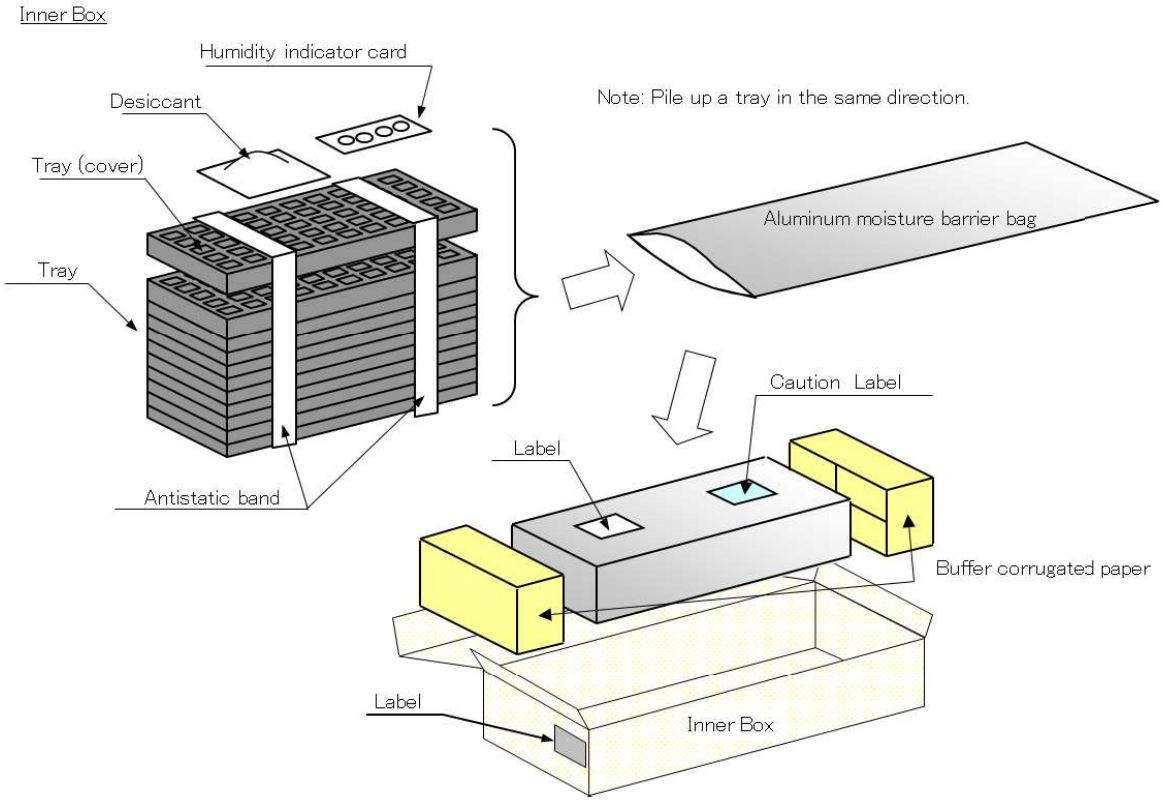


Figure35 package assembly

The entry item to a label is following.

- COMPANY NAME
- PRODUCT NAME CODE
- DESCRIPTION
- QUANTITY
- Lot No.
- NOTE

7.4. Recommended land dimensions

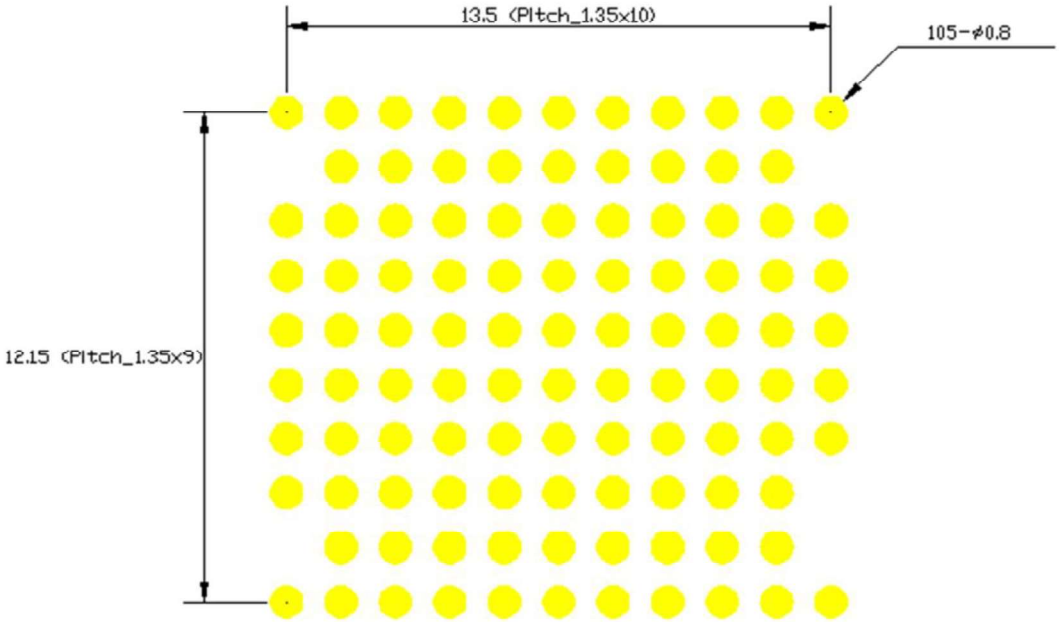


Figure36 Land dimensions of the module (unit: mm)

8. Handling Precautions

8.1. Thermal Management

WSCLxADAH2Z have high power consumption and due to their very small size, need to be designed properly for heat dissipation.

8.2. Desire and Conditions

This specification describes desire and conditions especially for mounting.

8.2.1. Environment conditions for use and storage

1. Store the components in an environment of < 40°C /90%RH if they are in a moisture barrier bag packed by TAIYO YUDEN.
2. Keep the factory ambient conditions at < 30°C /60%RH .
3. Store the components in an environment of < 25±5°C /10%RH after the bag is opened. (The condition is also applied to a stay in the manufacture process).

8.2.2. Conditions for handling of products

Make sure all of the moisture barrier bags have no holes, cracks or damages at receiving. If an abnormality is found on the bag, its moisture level must be checked in accordance with 2 of 8.2.2. Refer to the label on the bag.

1. All of the surface mounting process (reflow process) must be completed in 12 months from the bag sea date.
2. Make sure humidity in the bag is less than 10%RH immediately after open, using a humidity indicator card sealed with the components.
3. All of the surface mounting process (reflow process including rework process) must be completed in 168 hours after the bag is opened (inclusive of any other processes).
4. If any conditions in 8.2.1. or condition 2 and 3 of 8.2.2. are not met, bake the components in accordance with the conditions at 125°C 24h.
5. As a rule, baking the components in accordance with conditions 4 of 8.2.2. shall be once.
6. Since semi-conductors are inside of the components, they must be free from static electricity while handled. (<100V) Use ESD protective floor mats, wrist straps, ESD protective footwear, air ionizers etc., if necessary.
7. Please make sure that there are lessen mechanical vibration and shock for this module, and do not drop it.
8. Please recognize pads of back side at surface mount.
9. This module should not be cleaned.

10. Please perform temperature conditions of module at reflow within the limits of the following.
Please give the number of times of reflow as a maximum of 2 times.

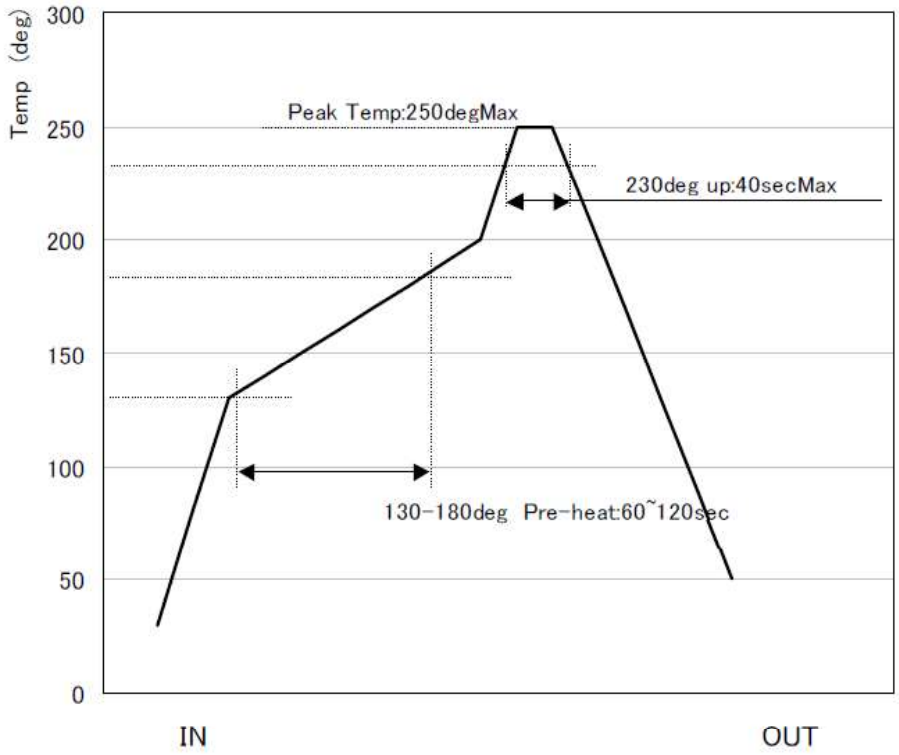


Figure37 temperature conditions of module at reflow

9. Certifications

9.1. Certifications

Table37 shows the certificate obtained by the module.

Table38 Product certifications

Certification	Model Name	
	WSCL2ADAH2Z	WSCL3ADAH2Z
technical regulations conformity certification of the Radio law	✔	✔
Japan Approvals institute for Telecommunications Equipment	✔	✔
Carrier IOT (docomo)	-	✔
Carrier IOT (kddi)	✔	–

10. Safety Information

Read the safety information carefully to ensure the correct and safe use of module. Applicable safety information must be observed.

10.1. Interference

Communication between this product and other might not be established nor maintained depending upon radio environment or operating condition of this product and other products with wireless technology.

This product operates in the licensed band at 2GHz/800MHz. In case this product is used around the other wireless devices which operate in same frequency band of this product, there is a possibility that interference occurs between this product and such other devices. If such interference occurs, please stop the operation of other devices or relocate this product before using this product or do not use this product around the other wireless devices.

Power off module if using the device is prohibited. Do not use the module when it causes danger or interference with electric devices.

10.2. Medical Device

- Power off module and follow the rules and regulations set forth by the hospitals and health care facilities.
- Some module may affect the performance of the hearing aids. For any such problems, consult your service provider.
- Pacemaker manufacturers recommend that a minimum distance of 15 cm be maintained between the module and a pacemaker to prevent potential interference with the pacemaker. If you are using an electronic medical device, consult the doctor or device manufacturer to confirm whether the radio wave affects the operation of this module.

10.3. Area with Inflammables and Explosives

To prevent explosions and fires in areas that are stored with inflammable and explosive devices, power off module and observe the rules. Areas stored with inflammables and explosives include but are not limited to the following:

- Gas station
- Fuel depot (such as the bunk below the deck of a ship)
- Container/Vehicle for storing or transporting fuels or chemical products
- Area where the air contains chemical substances and particles (such as granule, dust, or metal powder)
- Area indicated with the "Explosives" sign
- Area indicated with the "Power off bi-direction wireless equipment" sign
- Area where you are generally suggested to stop the engine of a vehicle

10.4. Airline Security

Observe the rules and regulations of airline companies. When boarding or approaching a plane, power off module. Otherwise, the radio signal of the module may interfere with the plane control signals.

10.5. Safety of Children

Do not allow children to use the module without guidance. Small and sharp components of the module may cause danger to children or cause suffocation if children swallow the components.

10.6. Environment Protection

Observe the local regulations regarding the disposal of your packaging materials, used module, and promote their recycling.

10.7. RoHS Approval

The module is in compliance with the restriction of the use of certain hazardous substances in electrical and electronic equipment Directive 2011/65/EU (RoHS Directive).

10.8. Laws and Regulations Observance

Observe laws and regulations when using module. Respect the privacy and legal rights of the others.

10.9. Care and Maintenance

It is normal that module gets hot when you use or charge it. Before you clean or maintain the module, stop all applications and power off the module.

- Use module with care and in clean environment. Keep the module from a fire or a lit cigarette.
- Protect module from water and vapor and keep it dry.
- Do not drop, throw or bend module.
- Clean module with a piece of damp and soft antistatic cloth. Do not use any chemical agents (such as alcohol and benzene), chemical detergent, or powder to clean it.
- Do not leave module in a place with a considerably low or high temperature.
- Do not dismantle the module. Otherwise, the module is not covered by the warranty.

10.10. Emergency Call

This module functions through receiving and transmitting radio signals.

Therefore, the connection cannot be guaranteed in all conditions. In an emergency, module cannot be used.

11. Appendix Acronyms and Abbreviations

Term	Definition
ADC	Analog-to-Digital Converter
AUX	auxiliary
DC	Direct Current
DH	Deep Hibernation
DRX	Discontinuous Reception
eDRX	Extended DRX
EJTAG	Embedded Joint Test Action Group
ESD	Electro-Static Discharge
EU	European Union
EUTRA	Evolved Universal Terrestrial Radio Access
FDD	Frequency Division Duplex
I2C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
LGA	Land Grid Array
LPDDR	Low Power DDR
LPF	Low-pass filter
LTE	Long Term Evolution
LwM2M	Lightweight machine-to-machine
MCP	Multi-chip Package
MISO	Master In Slave Out
MOSI	Master Out Slave In
NC	Not Connected
OFDM	Orthogonal Frequency Division Multiplexing
OFDMA	Orthogonal Frequency Division Multiple Access
PCB	Printed Circuit Board
PMU	Power Management Unit
PTW	Paging Transmission Window
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RoHS	Restriction of the Use of Certain Hazardous Substances
RRC	Radio Resource Control
RTC	Real Time Clock
Rx	Receive

SC-FDMA	Single-Carrier Frequency Division Multiple Access
SMS	Short Message Service
SPI	Serial Peripheral Interface
TCP	Transmission Control Protocol
TCXO	Temperature Compensated Crystal Oscillator
Tx	Transmit
UART	Universal Asynchronous Receiver Transmitter
UDP	User Datagram protocol
UICC	Universal Integrated Circuit Card
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module
UTRA	Universal Terrestrial Radio Access
XO	Crystal Oscillator. Typically used to indicate a Crystal connection to the IC (utilizing internal Oscillator)